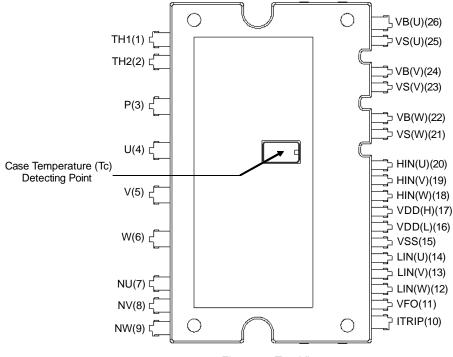


Integrated Power Functions

• 600 V – 15 A IGBT inverter for three–phase DC / AC power conversion (please refer to Figure 2)

Integrated Drive, Protection, and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting control circuit Under-Voltage Lock-Out Protection (UVLO) NOTE: Available bootstrap circuit example is given in Figure 13.
- For inverter low-side IGBTs: gate drive circuit, Short-Circuit Protection (SCP) control supply circuit Under-Voltage Lock-Out Protection (UVLO)
- Fault signaling: corresponding to UVLO (low-side supply) and SC faults
- Input interface: active–HIGH interface, works with 3.3 / 5 V logic, Schmitt–trigger input



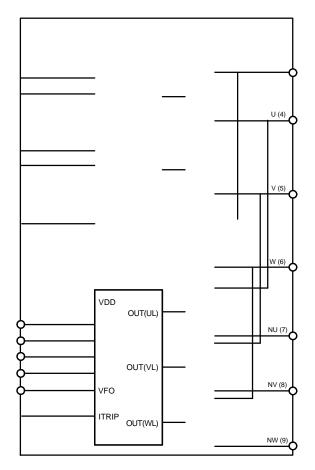
PIN CONFIGURATION

Figure 1. Top View

PIN DESCRIPTION

Pin No.	Pin Name	Description			
1	TH1	Thermistor Bias Voltage			
2	TH2	Series Resistor for the Use of Thermistor (Temperature Detection)			
3	Р	Positive DC-Link Input			
4	U	Output for U-Phase			
5	V	Output for V-Phase			
6	W	Output for W-Phase			
7	NU	Negative DC-Link Input for U-Phase			
8	NV	Negative DC-Link Input for V-Phase			
9	NW	Negative DC-Link Input for W-Phase			
10	ITRIP	Input for Current Protection			
11	VFO	Fault Output			
12	LIN(W)	Signal Input for Low-Side W-Phase			
13	LIN(V)	Signal Input for Low-Side V-Phase			
14	LIN(U)	Signal Input for Low–Side U–Phase			
15	VSS	Common Supply Ground			
16	VDD(L)	Low-Side Common Bias Voltage for IC and IGBTs Driving			
17	VDD(H)	High–Side Common Bias Voltage for IC and IGBTs Driving			
18	HIN(W)	Signal Input for High–Side W–Phase			
19	HIN(V)	Signal Input for High–Side V–Phase			
20	HIN(U)	Signal Input for High–Side U–Phase			
21	VS(W)	High–Side Bias Voltage Ground for W–Phase IGBT Driving			
22	VB(W)	High–Side Bias Voltage for W–Phase IGBT Driving			
23	VS(V)	High-Side Bias Voltage Ground for V-Phase IGBT Driving			
24	VB(V)	High-Side Bias Voltage for V-Phase IGBT Driving			
25	VS(U)	High-Side Bias Voltage Ground for U-Phase IGBT Driving			
26	VB(U)	High–Side Bias Voltage for U–Phase IGBT Driving			

nternal Equivalent Circuit and Input/Output Pins



NOTE:

- Inverter high-side is composed of three RC-IGBTs and one control IC for each IGBT.
 Inverter low-side is composed of three RC-IGBTs and one control IC for each IGBT. It has gate drive and protection functions.
- 3. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.

Figure 2. Internal Block Diagram

ABSOLUTE MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Rating	Unit
NVERTER F	ART		-	
VPN	Supply Voltage	P – NU, NV, NW	450	V
VPN(surge)	Supply Voltage (Surge)	P – NU, NV, NW	500	V
Vces	Collector – Emitter Voltage		600	V
±lc	Each IGBT Collector Current $Tc = 25^{\circ}C$		15	Α
±lcp	Each IGBT Collector Current (Peak)	Tc = 25°C, Under 1 ms Pulse Width 30		А
Pc	Collector Dissipation	$Tc = 25^{\circ}C$ Per One Chip (Note 4)	45	W
Tj	j Operating Junction Temperature		- 40~150	°C
CONTROL P	ART			
VDD	D Control Supply Voltage VDD(H), VDD(L) – VSS		20	V
VBS	High-Side Control Bias Voltage VB(U) - VS(U), VB(V) - VS(V), VB(W) - VS(W)		20	V
VIN	Input Signal Voltage	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) – VSS	-0.3~VDD + 0.3	V
VFO	Fault Output Supply Voltage	VFO – VSS	-0.3~VDD + 0.3	V
IFO	Fault Output Current	Sink Current at VFO pin	1	mA
VITRIP	Current-Sensing Input Voltage	ITRIP – VSS	-0.3~VDD + 0.3	V
BOOTSTRA	P DIODE PART	-	-	
VRRM	Maximum Repetitive Reverse Voltage		600	V
lf	Forward Current	Tc = 25°C	0.5	А
lfp	Forward Current (Peak)	Tc = 25° C, Under 1 ms Pulse Width (Note 4)		
Tj	Operating Junction Temperature		-40~150	°C
TOTAL SYST	rem	•		-
VPN(PROT)	Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability)	VDD = VBS = 13.5~16.5 V Tj = 150°C, Vces < 600 V Non-Repetitive, < 2 μs	400	V

	Protection Capability)	Non–Repetitive, < 2 μ s		
Tc	Module Case Operation Temperature	See Figure 1	-40~125	°C
Tstg	Storage Temperature		-40~125	°C
Viso	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate	2000	V _{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. These values had been made an acquisition by the calculation considered to design factor.

ABSOLUTE MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
THERMAL RESISTANCE						
Rth(j-c)Q	Junction to Case Thermal Resistance (Note 5)	Inverter IGBT Part (per 1/6 module)	-			

ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise noted)

Sy	mbol	Parameter	Conditions	Min	Тур	Max	Unit
INVE	INVERTER PART						
VCI	E(sat)	Collector-Emitter Saturation Voltage	VDD = VBS = 15 V, IN = 5 V, Ic = 15 A, Tj = 25°C	-	1.5	2.1	V
,	VF	FWDi Forward Voltage	IN = 0 V, Ic = -15 A, Tj = 25°C	-	1.75	2.35	V
HS	ton	Switching Times			0.75	-	μS
	tc(on)		Tj = 25°C, IN = 0 \leftrightarrow 5 V, Inductive Load (Note 6)	-	0.12	-	μS
	toff			-	0.85	-	
	-			-	-	-	
-							

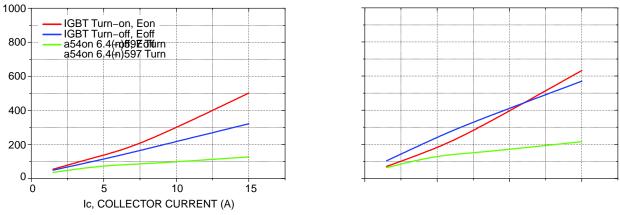




Figure 5. R-T Curve of The Built-In Thermistor

RECOMMENDED OPERATING CONDITIONS

Symbol Parameter Conditions Min Typ Max Unit
--

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions		Min	Тур	Max	Unit
Device Flatness	See Figure 7		0	-	+120	μm
Mounting Torque	Mounting Screw: M3	Recommended 0.7 N · m	0.6	0.7	0.8	N·m
	See Figure 8 Recommended 7.1 kg · cm		6.2	7.1	8.1	kg∙cm
Weight		-	11.00	-	g	

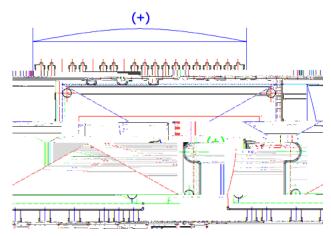


Figure 7. Flatness Measurement Position

Figure 8. Mounting Screws Torque Order

Time Charts of Protective Function

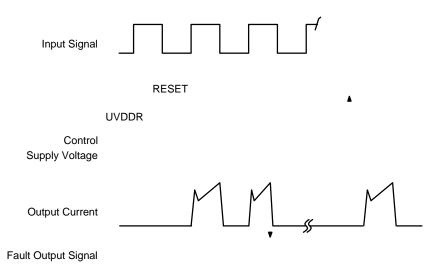
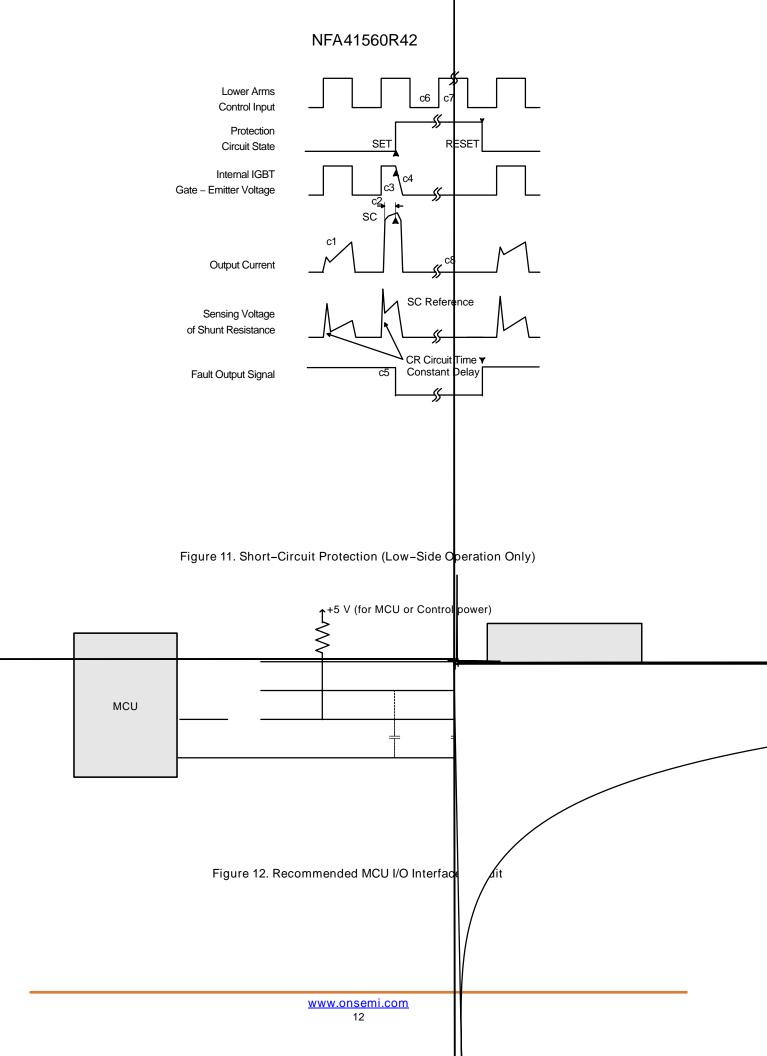


Figure 9. Under-Voltage Protection (Low-Side)

Figure 10. Under-Voltage Protection (High-side)



NOTE:

- 14. To avoid malfunction, the wiring of each input should be as short as possible (less than 2 3 cm).
- 15. VFO output is open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes IFO up to 1 mA.
- 16. Input signal is active–HIGH type. There is a $5k\Omega$ resistor inside the IC to pull down each input signal line to GND. RC coupling circuits is recommended for the prevention of input signal oscillation. R1C1 time constant should be selected in the range 50~150 ns (recommended R1 = 100 Ω , C1 = 1 nF).
- 17. Each wiring pattern inductance of point A should be minimized (recommend less than 10 nH). Use the shunt resistor R3 of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point E should be connected to the terminal of the shunt resistor R3 as close as possible.
- 18. To insert the shunt resistor to measure each phase current at NU, NV, NW terminal, it makes to change the trip level ISC about the short-circuit current.

Figure 13. Typical Application Circuit

ORDERING INFORMATION

Device	Device Marking	Package	Shipping
NFA41560R42	NFA41560R42	SPMAA-C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE (Pb-Free)	12 Units / Rail

SPM is registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. Onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or incruit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi