## Features

- 1200 V 35 A 3−Phase FS7 IGBT Inverter, Including Control ICs for Gate Drive and Protections
- Very Low Thermal Resistance Using Al2O3 DBC Substrate
- Active Logic Interface
- Built−in Under−voltage Protection (UVP)
- Built−In Bootstrap Diodes/Resistors
- Separate Low−side IG0031 Tc(BuoqBitter Connections for Individual Curren1 Tf6 1124 1.258 Tc(sideate Lownsing of Each PhaseTf12 0

©

Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built−in IGBTs to minimize EMI and losses, while also providing multiple on−module protection features including under−voltage lockouts, over−current shutdown, thermal monitoring of drive IC, and fault reporting. The built−in, high−speed

# NFAM3512L7B

**PIN DESCRIPTION**

| Pin | Name | Description |
|---|---|---|
| 1 | VS(U) | High−Side Bias Voltage GND for U Phase IGBT Driving |
| (2) | − | Dummy |
| 3 | VB(U) | High−Side Bias Voltage for U Phase IGBT Driving |
| 4 | VDD(UH) | High−Side Bias Voltage for U Phase IC |
| (5) | − | Dummy |
| 6 | HIN(U) | Signal Input for High−Side U Phase |
| 7 | VS(V) | High−Side Bias Voltage GND for V Phase IGBT Driving |
| (8) | − | Dummy |
| 9 | VB(V) | High−Side Bias Voltage for V Phase IGBT Driving |
| 10 | VDD(VH) | High−Side Bias Voltage for V Phase IC |
| (11) | − | Dummy |
| 12 | HIN(V) | Signal Input for High−Side V Phase |
| 13 | VS(W) | High−Side Bias Voltage GND for W Phase IGBT Driving |
| (14) | − | Dummy |
| 15 | VB(W) | High−Side Bias Voltage for W Phase IGBT Driving |
| 16 | VDD(WH) | High−Side Bias Voltage for W Phase IC |
| (17) | − | Dummy |
| 18 | HIN(W) | Signal Input for High−Side W Phase |
| (19) | − | Dummy |
| 20 | VTS | |

## Internal Equivalent Circuit and Input/Output Pins

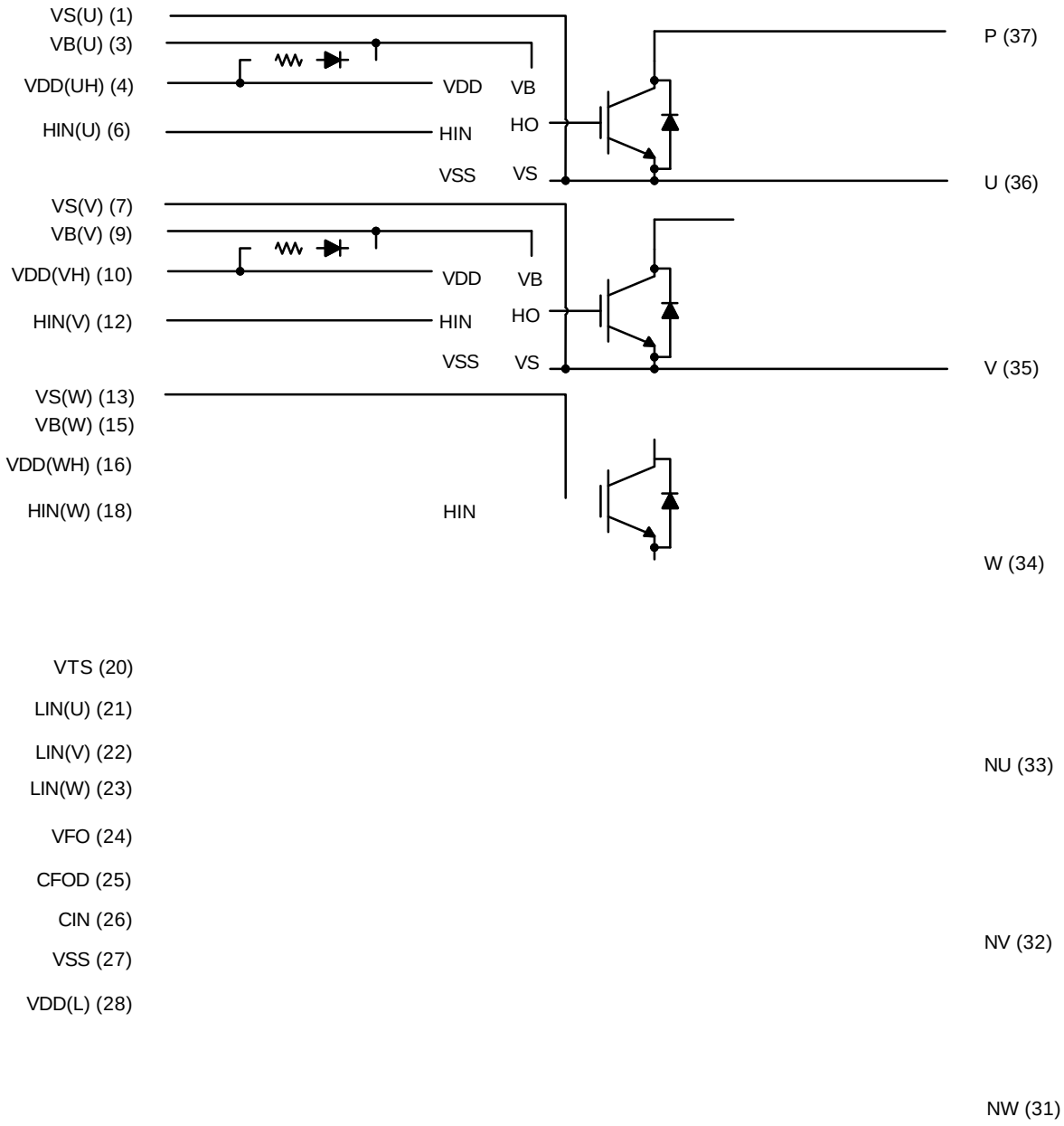



**Figure 2. Internal Block Diagram**

**ABSOLUTE MAXIMUM RATINGS** (VDD = 15 V and Tj = 25°C, Unless Otherwise Specified)

| Symbol | Parameter | Test Condition | Max | Unit |
|---|---|---|---|---|
| **INVERTER PART** | | | | |
| VPN | Supply Voltage | Applied between P − NU, NV, NW | 900 | V |
| VPN (surge) | Supply Voltage (Surge) | Applied between P − NU, NV, NW (Note 1) | 1000 | V |
| Vces | Collector − Emitter Voltage | | 1200 | V |
| VRRM | Maximum Repetitive Reverse Voltage | | 1200 | V |
| ± Ic | Each IGBT Collector Current | | 35 | A |
| ± Icp | Each IGBT Collector Current (Peak) | Tc = 25°C, Tj ≤ 150°C, under 1 ms Pulse Width | 70 | A |
| Pc | Collector Dissipation | Tc = 25°C per one chip (Note 2) | 167 | W |
| Tj | Operating Junction Temperature | | −40 ~ 150 | °C |
| **CONTROL PART** | | | | |
| VDD | Control Supply Voltage | Applied between VDD(H), VDD(L) − VSS | 20 | V |
| VBS | High−Side Control Bias Voltage | Applied between VB(U) – VS(U),<br>VB(V) – VS(V), VB(W) – VS(W) | 20 | V |
| VIN | Input Signal Voltage | Applied between HIN(U), HIN(V), HIN(W),<br>LIN(U), LIN(V), LIN(W) − VSS | −0.3 ~ VDD + 0.3 | V |
| VFO | Fault Output Supply Voltage | Applied between VFO – VSS | −0.3 ~ VDD + 0.3 | V |
| IFO | Fault Output Current | Sink Current at VFO pin | 2 | mA |
| VCIN | Current Sensing Input Voltage | Applied between CIN − VSS | −0.3 ~ VDD + 0.3 | V |
| **TOTAL SYSTEM** | | | | |
| VPN(PROT) | Self−Protection Supply Voltage Limit<br>(Short Circuit Protection Capability) | VDD = VBS = 13.5 ~ 16.5 V, Tj = 150°C,<br>Non−repetitive, < 2μs | 800 | V |
| Tc | Case Operation Temperature | See Figure 1 | −40 ~ 125 | °C |
| Tstg | Storage Temperature | | −40 ~ 125 | °C |
| Viso | Isolation Voltage | 60 Hz, Sinusoidal, AC 1 minute,<br>Connection Pins to Heat Sink Plate | 2500 | $V_{rms}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminal.
2. Calculation value considered to design factor.

**THERMAL RESISTANCE**

| Symbol | Rating | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Rth(j−c)Q | Junction to Case Thermal Resistance (Note 3) | Inverter IGBT Part (per 1/6 Module) | − | − | 0.75 | °C/W |
| Rth(j− | | | | | | |

**ELECTRICAL CHARACTERISTICS** (VDD = 15 V and Tj = 25°C, Unless Otherwise Specified)

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INVERTER PART** | | | | | | |
| Ices | Collector − Emitter Leakage Current | Tj = 25°C, Vce = Vces | − | − | 1 | mA |
| | | Tj = 150°C, Vce = Vces | − | − | 10 | mA |

VCE(sat3−66.0703.5938 670.9601 0 0 8 450.5n.e6a .9071 ref4.375a1c7.32 680.882 .90707 14.4 ref467.32 693 666.0703.5938 670.96011or Leakage Current

# NFAM3512L7B

## Typical Application Circuit

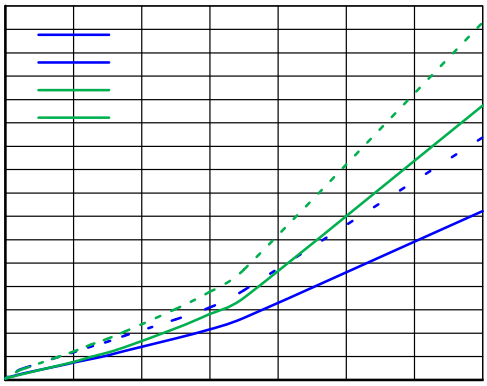
Input Signal

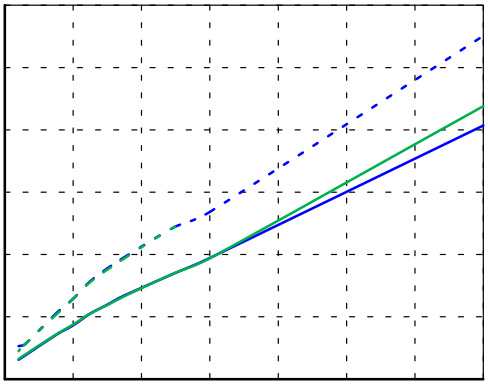
To avoid malfunction, the wiring of each input should be as short as possible (less than 2−3 cm). Each capacitor should be mounted as close to the pins of the product as possible. VFO output is open−drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes IFO up to 1 mA. Please refer to Figure 5.

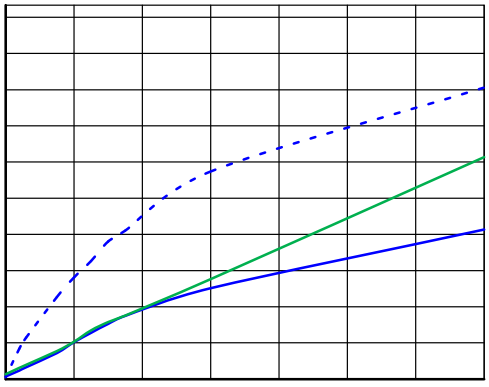
NOTES:

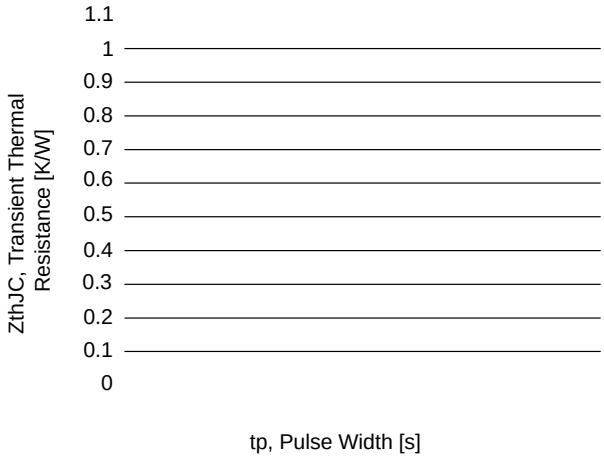
9. Input signal is active−HIGH type. There is a 5 kΩ resistor inside the IC to pull−down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. RC time constant should be selected in the range 50 ~ 150 ns. (Recommended R = 100 Ω , C = 1 nF)
10. Each wiring pattern inductance should be minimized (Recommend less than 10 nH). Use the shunt resistor of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring should be connected to the terminal of the shunt resistor as close as possible.
11. In the short−circuit protection circuit, please select the RC time constant in the range 1.5 ~ 2 μs. Do enough evaluation on the real system because short−circuit protection time may vary wiring pattern layout and value of the RC time constant.
12. To prevent surge destruction, the wiring between the snubber capacitor and the P & GND pins should be as short as possible. The use of a high−frequency non−inductive capacitor of around 0.1 ~ 0.22 μF between the P & GND pins is recommended.
13. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (Recommended zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15 Ω).
14. VDD electrolytic capacitor is recommended around 7 times larger than VBS electrolytic bootstrap capacitor.
15. Please choose the VBS electrolytic bootstrap capacitor with good temperature characteristic.
16. 0.1 ~ 0.2 μF R−category ceramic capacitors with good temperature and frequency characteristics is recommended.
17. Fault out pulse width can be adjusted by capacitor connected to the CFOD terminal.
18. To prevent protection function errors, CIN capacitor should be placed as close to CIN and VSS pins as possible.

**Figure 10. Typical Application Circuit**








1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
ZthJC, Transient Thermal Resistance [K/W]
tp, Pulse Width [s]

# NFAM3512L7B

CASE MODGX
ISSUE A

DATE 20 DEC 2023

XXXXX = Specific Device Code
ZZZ = Assembly Lot Code
AT = Assembly & Test Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪

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