Intelligent Power Module (IPM), 650 V, 50 A

Advanced

NFAM5065L4BL

DIP39, 54.5x31.0 EP
CASE MODGX

General Description

The NFAM5065L4BL is a fully-integrated inverter power module consisting of an independent High side gate driver, LVIC, six IGBT's and a temperature sensor (VTS), suitable for driving permanent magnet synchronous (PMSM) motors, brushless DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a three-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.

The power stage has under voltage lockout protection (UVP). Internal boost diodes are provided for high side gate boost drive.

Features

- Three-phase 650 V, 50 A IGBT Module with Independent DriversFeatures

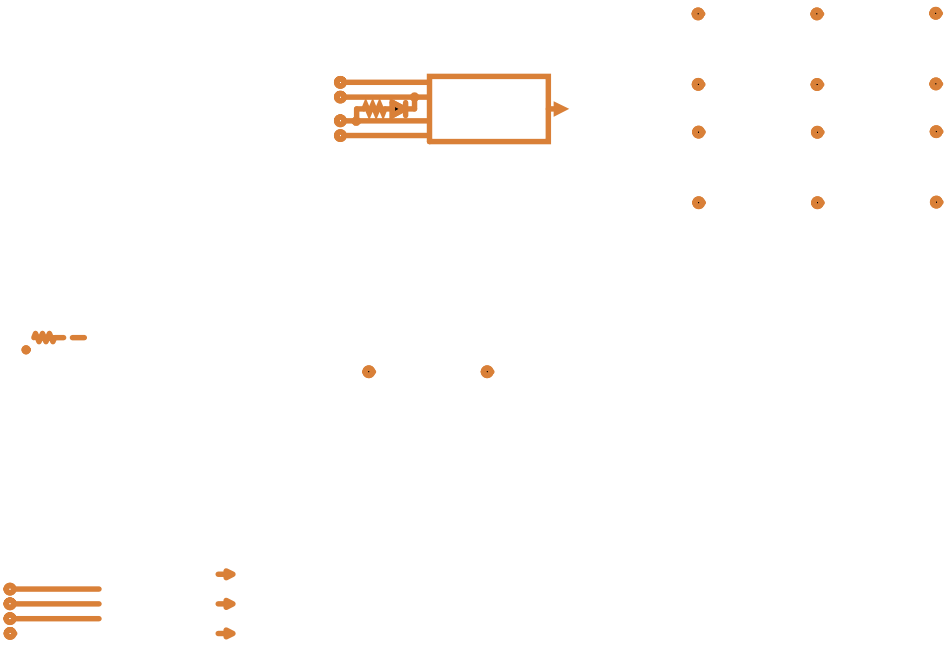
MARKING DIAGR

Device marking is on packag

NFAM5065L4BL	= Specific De
ZZZ	= Assembly L
A	= Assembly L
T	= Test Locatio
Y	= Year
WW	= Work Week

ORDERING INFORMA

Device	Package
NFAM5065L4BL	DIP39 54.5 x 31.0 (Pb-Free)



BLOCK DIAGRAM

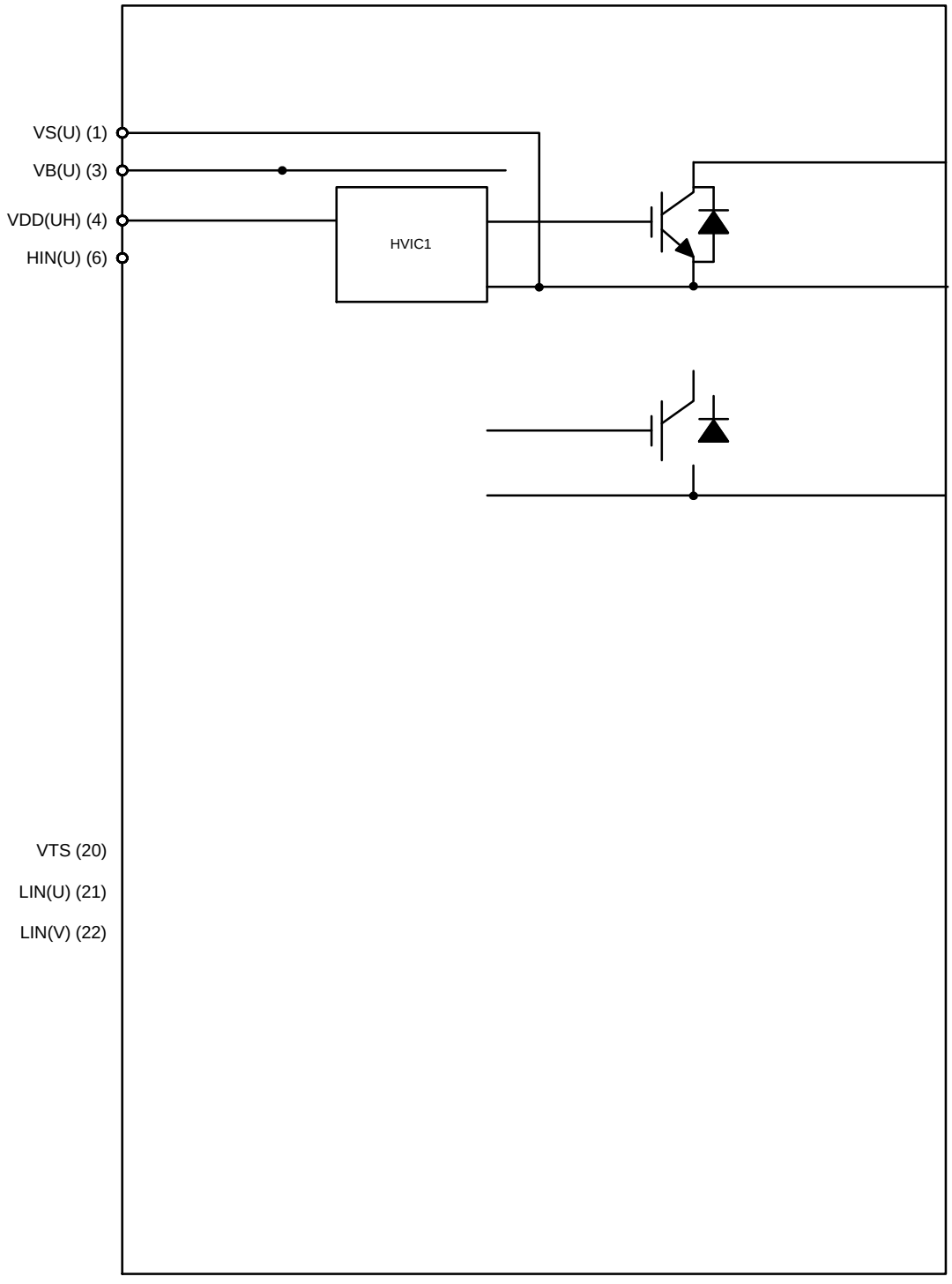


Figure 3. Equivalent Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	VS(U)	High−Side Bias Voltage GND for U phase IGBT Driving
(2)	−	Dummy
3	VB(U)	High−Side Bias Voltage for U phase IGBT Driving
4	VDD(UH)	High−Side Bias Voltage for U phase IC
(5)	−	Dummy
6	HIN(U)	Signal Input for High−Side U Phase
7	VS(V)	High−Side Bias Voltage GND for V phase IGBT Driving
(8)	−	Dummy
9	VB(V)	High−Side Bias Voltage for V phase IGBT Driving
10	VDD(VH)	High−Side Bias Voltage for V phase IC
(11)	−	Dummy
12	HIN(V)	Signal Input for High−Side V Phase
13	VS(W)	High−Side Bias Voltage GND for W phase IGBT Driving
(14)	−	Dummy
15	VB(W)	High−Side Bias Voltage for W phase IGBT Driving
16	VDD(WH)	High−Side Bias Voltage for W phase IC
(17)	−	Dummy
18	HIN(W)	Signal Input for High−Side W Phase
(19)	−	Dummy
20	VTS	Voltage Output for LVIC Temperature Sensing Unit
21	LIN(U)	Signal Input for Low−Side U Phase
22	LIN(V)	Signal Input for Low−Side V Phase
23	LIN(W)	Signal Input for Low−Side W Phase
24	VFO	Fault Output
25	CFOD	Capacitor for Fault Output Duration Selection
26	CIN	Input for Current Protection
27	VSS	Low−Side Common Supply Ground
28	VDD(L)	Low−Side Bias Voltage for IC and IGBTs Driving
(29)	−	Dummy
(30)	−	Dummy
31	NW	Negative DC−Link Input for U Phase
32	NV	Negative DC−Link Input for V Phase
33	NU	Negative DC−Link Input for W Phase
34	W	Output for U Phase
35	V	Output for V Phase
36	U	Output for W Phase
37	P	Positive DC−Link Input
38	N.C	No Connection
(39)	−	Dummy

1. Pins of () are the dummy for internal connection. These pins should be no connection.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C) (Note 2)

Symbol	Rating	Conditions	Value	Unit
VPN	Supply Voltage	P−NU, NV, NW	450	V
VPN(surge)	Supply Voltage (Surge)	P−NU, NV, NW (Note 3)	550	V
VPN(PROT)	Self Protection Supply Voltage Limit (Short−Circuit Protection Capability)	VDD = VBS = 13.5 V ~16.5 V, T_J = 150°C,		

RECOMMENDED OPERATING CONDITIONS (Note 5)

Symbol	Rating	Conditions		Min	Typ	Max	Unit
VPN	Supply Voltage	P−NU, NV, NW		−	300	400	V
VDD	Gate Driver Supply Voltages	VDD(UH,VH,WH), VDD(L)−VSS		13.5	15	16.5	V
VBS		VB(U)−VS(U), VB(V)−VS(V), VB(W)−VS(W)		13.0	15	18.5	V
dVDD / dt, dVBS / dt	Supply Voltage Variation			−1	−	1	V/μs
fPWM	PWM Frequency			1	−	20	kHz
DT	Dead Time	Turn-off to Turn-on (external)		2.0	−	−	μs
Io	Allowable r.m.s. Current	VPN = 300 V, VDD = 15 V, P.F. = 0.8 Tc ≤ 125°C, Tj ≤ 150°C (Note 5)	f_{PWM} = 5 kHz	−	−	29.2	Arms
			f_{PWM} = 15 kHz	−	−	20.2	
PWIN (on)	Allowable Input Pulse Width	200 V ≤ VPN ≤ 400 V 13.5 V ≤ VDD ≤ 16.5 V 13.0 V ≤ VBS ≤ 18.5 V −20°C ≤ Tc ≤ 100°C		1.0	−	−	μs
PWIN (off)				1.5	−	−	
	Package Mounting Torque	M3 type screw		0.6	0.7	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Allowable r.m.s current depends on the actual conditions.
6. Flatness tolerance of the heatsink should be within −50 μm to +100 μm.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, VDD = 15 V, VBS = 15 V, unless otherwise specified.) (Note 7)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
INVERTERSECTION							
Ices	Collector-Emitter Leakage Current		Vce = Vces, T_J = 25°C	−	−	1	mA
			Vce = Vces, T_J = 150°C	−	−	10	mA
VCE(sat)	Collector-Emitter Saturation Voltage		VDD = VBS = 15 V, IN = 5 V Ic = 50 A, T_J = 25°C	−	1.65	2.30	V
			VDD = VBS = 15 V, IN = 5 V Ic = 50 A, T_J = 150°C	−	1.85	−	V
VF	FWDi Forward Voltage		IN = 0 V, Ic = 50 A, T_J = 25°C	−	2.00	2.40	V
			IN = 0 V, Ic = 50 A, T_J = 150°C	−	2.00	−	V
ton	Switching Times	High Side	VPN = 300 V, VDD(H) = VDD(L) = 15 V Ic = 50 A, T_J = 25°C, IN = 0 ⇔ 5 V Inductive Load	1.05	1.65	2.25	μs
tc(on)				−	0.40	0.90	μs
toff				−	1.80	2.40	μs
tc(off)				−	0.25	0.75	μs
trr				−	0.25	−	μs
ton		Low Side	VPN = 300 V, VDD(H) = VDD(L) = 15 V Ic = 50 A, T_J = 25°C, IN = 0 ⇔ 5 V Inductive Load	1.25	1.85	2.45	μs
tc(on)				−	0.50	1.00	μs
toff				−	1.70	2.30	μs
tc(off)				−	0.25	0.75	μs
trr				−	0.25	−	μs

ELECTRICAL CHARACTERISTICS (T_C = 25°C, VDD = 15 V, VBS = 15 V, unless otherwise specified.) (Note 7) (continued)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
DRIVER SECTION							
IQDDH	Quiescent VDD Supply Current	VDD(UH,VH,WH) = 15 V, HIN(U,V,W) = 0 V	VDD(UH)−VSS VDD(VH)−VSS VDD(WH)−VSS	−	−	0.30	mA
IQDDL		VDD(L) = 15 V, LIN(U,V,W) = 0 V	VDD(L)−VSS	−	−	3.50	mA
IPDDH	Operating VCC Supply Current	VDD(UH,VH,WH) = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for High-Side	VDD(UH)−VSS VDD(VH)−VSS VDD(WH)−VSS	−	−	0.40	mA
IPDDL		VDD(L) = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for Low-Side	VDD(L)−VSS	−	−	6.00	mA
IQBS	Quiescent VBS Supply Current	VBS = 15 V, HIN(U,V,W) = 0 V	VB(U)−VS(U) VB(V)−VS(V) VB(W)−VS(W)	−	−	0.30	mA
IPBS	Operating VBS Supply Current	VDD = VBS = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for High-Side	VB(U)−VS(U) VB(V)−VS(V) VB(W)−VS(W)	−	−	5.00	mA
VIN(ON)	ON Threshold Voltage	HIN(U,V,W)−VSS, LIN(U,V,W)−VSS		−	−	2.6	V
VIN(OFF)	OFF Threshold Voltage			0.8	−	−	V
VCIN(ref)	Short Circuit Trip Level	VDD = 15 V, CIN−VSS		0.46	0.48	0.50	V
UVDDD	Supply Circuit Under-Voltage Protection	Detection Level		10.3	−	12.5	V
UVDDR		Reset Level		10.8	−	13.0	V
UVBSD		Detection Level		10.0	−	12.0	V
UVBSR		Reset Level		10.5	−	12.5	V
VTS	Voltage Output for LVIC Temperature Sensing Unit	VTS−VSS = 10 nF, Temp. = 25°C		0.905	1.030	1.155	V
VFOH	Fault Output Voltage	VDD = 0 V, CIN = 0 V, VFO Circuit: 10 kΩ to 5 V Pull-up		4.9	−	−	V
VFOL		VDD = 0 V, CIN = 1 V, VFO Circuit: 10 kΩ to 5 V Pull-up		−	−	0.95rR5u6T452.976 28iw4 18 0 0	

Temperature of LVIC versus VTS Characteristics

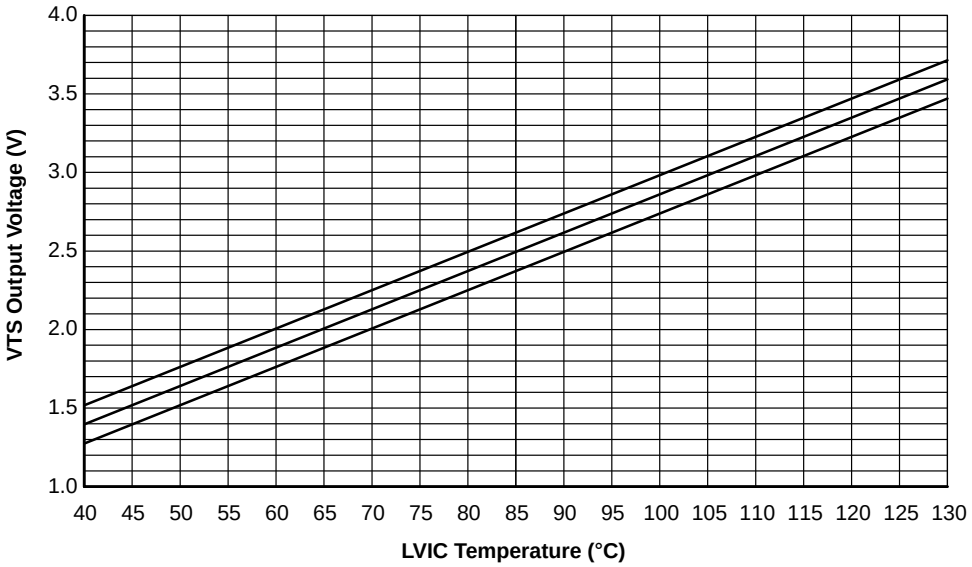
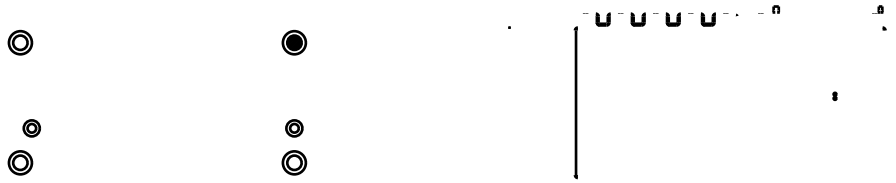


Figure 4. Temperature of LVIC versus VTS Characteristics

CASE MODGX
ISSUE A

DATE 20 DEC 2023



XXXXX = Specific Device Code
ZZZ = Assembly Lot Code
AT = Assembly & Test Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪