Inverter, 1200 V, 40 A

A 5312

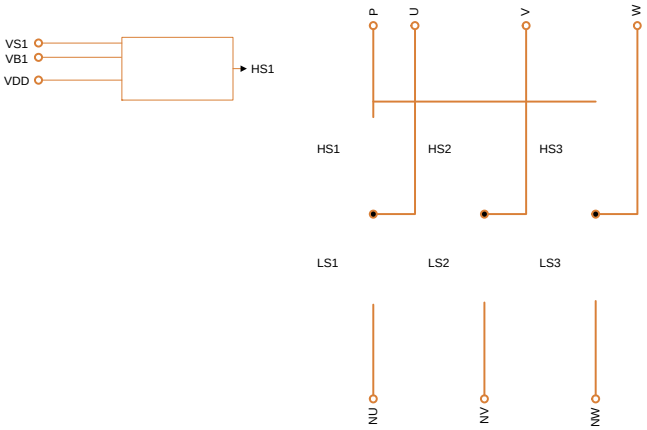
General Description

The NFAM5312SCBUT is a fully−integrated inverter power module consisting of an independent High side gate driver, LVIC, six SiC MOSFET’s and a temperature sensor (VTS or Thermistor), suitable for driving permanent magnet synchronous (PMSM) motors, brushless DC (BLDC) motors and AC asynchronous motors. The MOSFET’s are configured in a three−phase bridge with separate source connections for the lower legs for maximum flexibility in the choice of control algorithm.

The power stage has undervoltage lockout protection (UVP). Internal bootstrap diodes/resistors are provided for high side control.

Features

- 1200 V 40 A 3−Phase MOSFET Inverter, Including Control ICs for Gate Drive and Protections
- Active Logic Interface
- Built−in Under Tc80ef1fTMT6TT6At9 0 TD-004 Tc(in Under Tc80ef1fTMT6TT6At9 Control ICse1rest)e



- Built−inBbootstrapDdiodesRresistore
-

PIN DESCRIPTION

Pin	Name	Description
1	VS(U)	High−Side Bias Voltage Ground for U−Phase MOSFET Driving
(2)	−	Dummy
3	VB(U)	High−Side floating supply voltage for U−Phase MOSFET Driving
4	VDD(UH)	High−Side control power supply for U−Phase IC
(5)	−	Dummy
6	HIN(U)	Signal Input for High−Side U−Phase
7	VS(V)	High−Side Bias Voltage Ground for V−Phase MOSFET Driving
(8)	−	Dummy
9	VB(V)	High−Side floating supply voltage for V−Phase MOSFET Driving
10	VDD(VH)	High−Side control power supply for V−Phase IC
(11)	−	Dummy
12	HIN(V)	Signal Input for High−Side V−Phase
13	VS(W)	High−Side Bias Voltage Ground for W−Phase MOSFET Driving
(14)	−	Dummy
15	VB(W)	High−Side floating supply voltage for W−Phase MOSFET Driving
16	VDD(WH)	High−Side control power supply for W−Phase IC
(17)	−	Dummy
18	HIN(W)	Signal Input for High−Side W−Phase
(19)	−	Dummy
20	VTS	Output for LVIC Temperature Sensing Voltage
21	LIN(U)	Signal Input for Low−Side U−Phase
22	LIN(V)	Signal Input for Low−Side V−Phase
23	LIN(W)	Signal Input for Low−Side W−Phase
24	VFO	Fault Output
25	CFOD	Capacitor for Fault Output Duration Selection
26	CIN	Input for Current Protection
27	VSS	Low−Side Common Supply Ground
28	VDD(L)	Low−Side Bias Voltage for IC and MOSFETs Driving
(29)	−	Dummy
(30)	−	Dummy
31	NW	Negative DC−Link Input for W−Phase
32	NV	Negative DC−Link Input for V−Phase
33	NU	Negative DC−Link Input for U−Phase
34	W	Output for W−Phase
35	V	Output for V−Phase
36	U	Output for U−Phase
37	P	Positive DC−Link Input
38	TH1	Thermistor connection (T) / No connection
39	TH2	Thermistor connection *optional for T

NOTE: Pins of ( ) are the dummy for internal connection. These pins should be no connection.

INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS

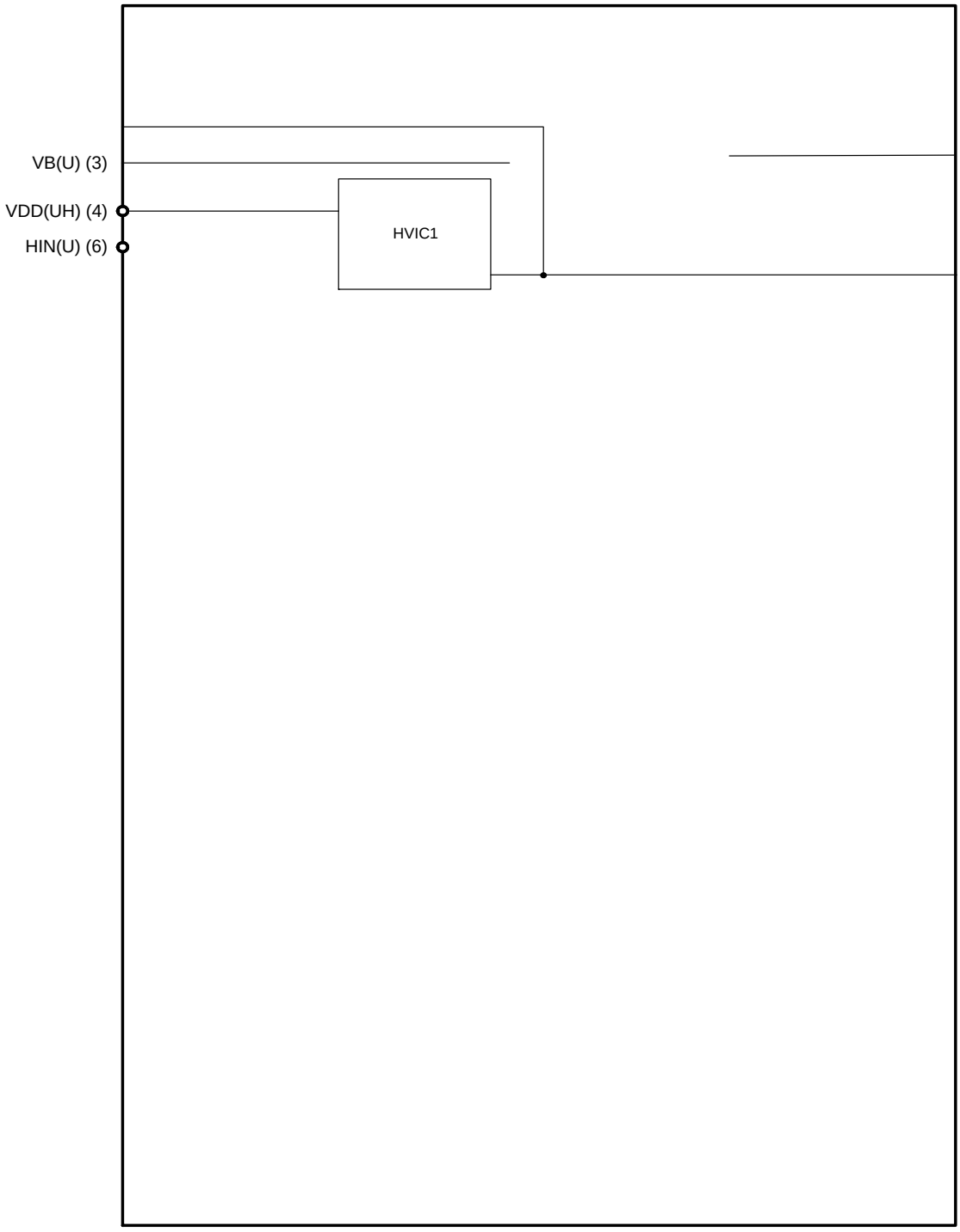


Figure 3. Internal Block Diagram

ELECTRICAL CHARACTERISTICS (Tc = 25°C, VDD = 18 V, VBS = 18 V, unless otherwise noted) (Notes 8, 9)

Symbol	Description	Conditions		Min	Typ	Max	Unit
INVERTER PART							
IDSS	Drain – Source Leakage Current	VDS = 1200 V, Tj = 25°C		–	–	1	mA
		VDS = 1200 V, Tj = 150°C		–	–	10	mA
RDS(ON)	Drain to Source On Resistance	ID = 40 A, VDD = VBS = 18 V, Tj = 25°C		–	53	72	mΩ
		ID = 40 A, VDD = VBS = 18 V, Tj = 150°C		–	97	–	mΩ
VSD	Diode Forward Voltage	VDD = VBS = 18 V, ISD = 40 A, Tj = 25°C	HIN/LIN = OFF	–	4.80	5.50	V
			HIN/LIN = ON	–	1.70	2.35	V
		VDD = VBS = 18 V, HIN/LIN = ON, ISD = 40 A, Tj = 150°C	HIN/LIN = OFF	–	5.15	–	V
			HIN/LIN = ON	–	3.10	–	V

ELECTRICAL CHARACTERISTICS (Tc = 25°C, VDD = 18 V, VBS = 18 V, unless otherwise noted) (Notes 8, 9)

Symbol	Description	Conditions	Min	Typ	Max	Unit
CONTROL PART						
UVBSD	Supply Circuit Under−Voltage Protection	VBS supply undervoltage negative going input threshold	10.0	−	12.0	V
UVBSR		VBS supply undervoltage positive going input threshold	10.5	−	12.5	V
VTS	Voltage Output for LVIC Temperature Sensing Unit	Pull down R = 5.1 kΩ, Temp. = 85°C	2.50	2.63	2.76	V
VFOH	Fault Output Voltage	VDD(L) = 0 V, CIN = 0 V, VFO Circuit: 10 kΩ to 5 V Pull−up	4.9	−	−	V
VFOL		VDD(L) = 0 V, CIN = 1 V, VFO Circuit: 10 kΩ to 5 V Pull−up	−	−	0.95	V
tFOD	Fault−Out Pulse Width	CFOD = 22 nF (Note 6)	1.6	2.2	−	ms
BOOTSTRAP PART						
VF BD	Bootstrap Diode Forward Current	If = 0.1 A (See Figure 7)	2.1	2.5	2.9	V
R BOOT	Built−in Limiting Resistance		12.5	15.5	18.5	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES: Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at Tj = Ta = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible. Values based on design and/or characterization.

4. ton and toff include the propagation delay of the internal drive IC. tc(on) and tc(off) are the switching times of MOSFET under the given gate−driving condition internally. For the detailed information, please see Figure 4.

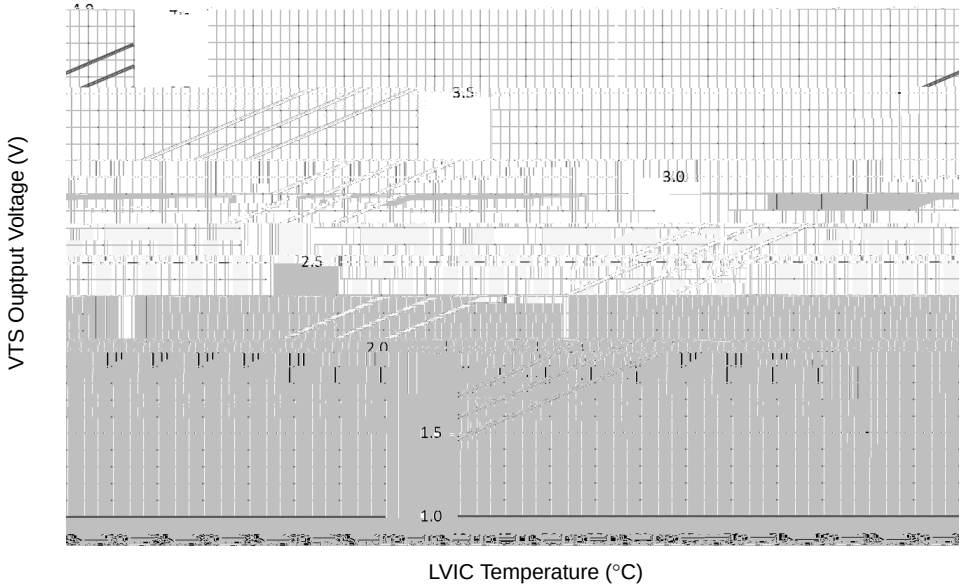


Figure 5. Temperature of LVIC versus VTS Characteristics

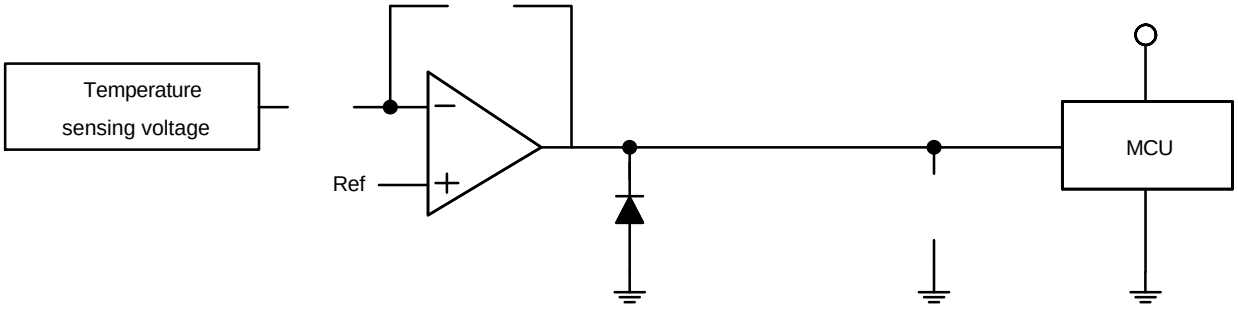


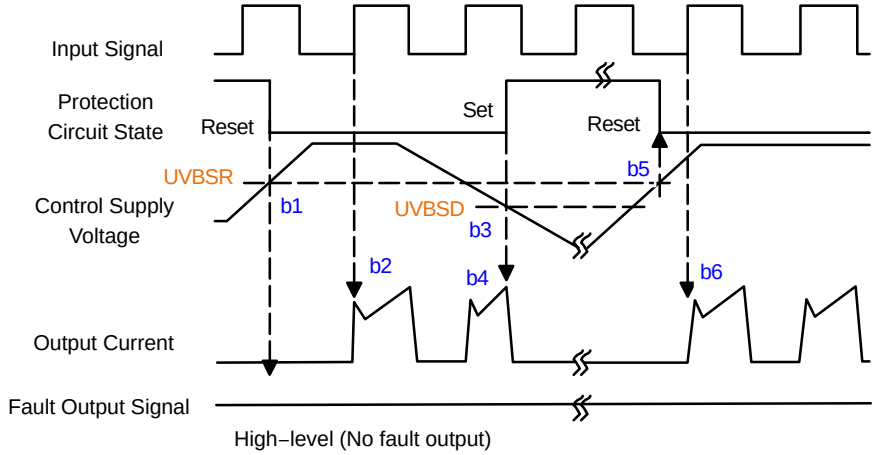
Figure 6. Internal Block Diagram and Interface Circuit of VTS

THERMISTOR CHARACTERISTICS (Included only in NFAM5312SCBUT)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	46.530	47	47.47	kΩ
Resistance	R_{125}	Tc = 100°C	1.344	1.406	1.471	kΩ

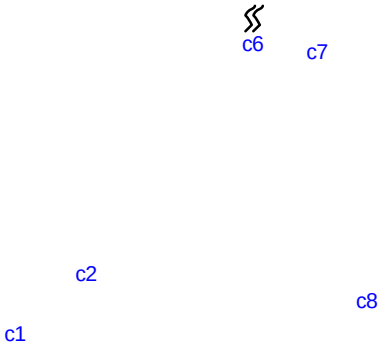
RECOMMENDED OPERATING CONDITIONS

Symbol	Rating	Conditions	Min	Typ	Max	Unit
VPN	Supply Voltage	Applied between P – NU, NV, NW	–	600	800	V
VDD	Control Supply Voltage	Applied between VDD(H) – VSS, VDD(L) – VSS	13.0	18.0	19.0	V
VBS	High−Side Bias Voltages	Applied between VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)	13.5	18.0	19.5	V
dVDD / dt dVBSt						



b1 : Control supply voltage rises: After the voltage reaches UVBSR, the circuits start to operate when next input is applied.
b2 : Normal operation: MOSFET ON and carrying current.
b3 : Under voltage detection (UVBSD).
b4 : MOSFET OFF in spite of control input condition, but there is no fault output signal.
b5 : Under voltage reset (UVBSR).
b6 : Normal operation: MOSFET ON and carrying current by triggering next signal from LOW to HIGH.

Figure 10. Under−Voltage Protection (High−Side)



(with the external sense resistance and RC filter connection)
c1 : Normal operation: MOSFET ON and carrying current.
c2 : Short circuit current detection (SC trigger).
c3 : All low−side MOSFET's gate are hard interrupted.
c4 : All low−side MOSFET's turn OFF.
c5 : Fault output operation starts with a fixed pulse width.
c6 : Input HIGH: MOSFET ON state, but during the active period of fault output the MOSFET doesn't turn ON.
c7 : Fault output operation finishes, but MOSFET doesn't turn on until triggering next signal from LOW to HIGH.
c8 : Normal operation: MOSFET ON and carrying current.

Figure 11. Short−Circuit Current Protection (Low−Side Operation only)

TYPICAL APPLICATION CIRCUIT

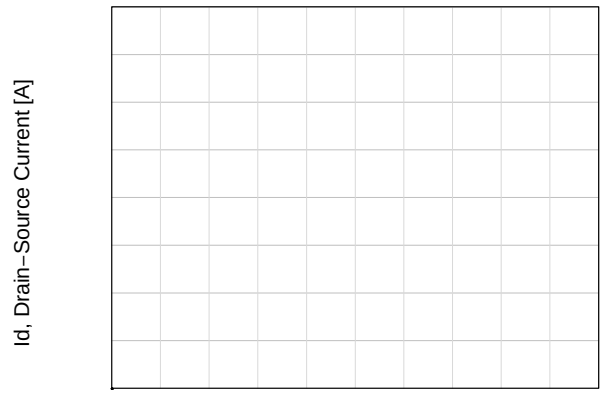


Figure 13. Typ. Drain−Source Saturation Voltage

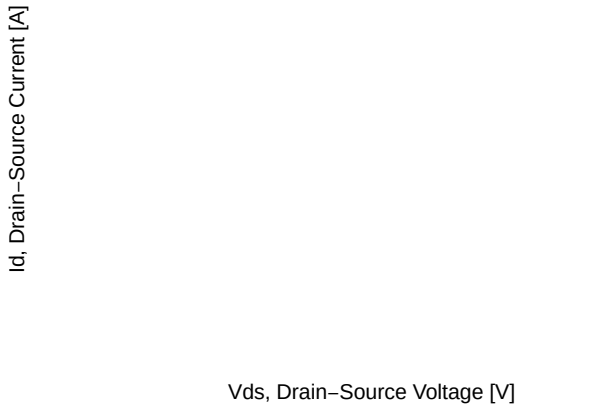


Figure 14. Drain−Source Saturation Voltage

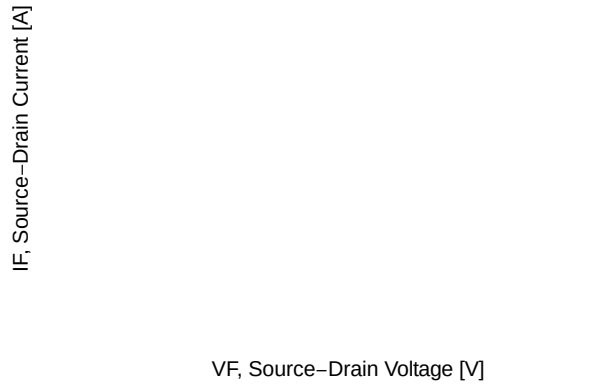


Figure 15. Typ. Source−Drain Forward Voltage

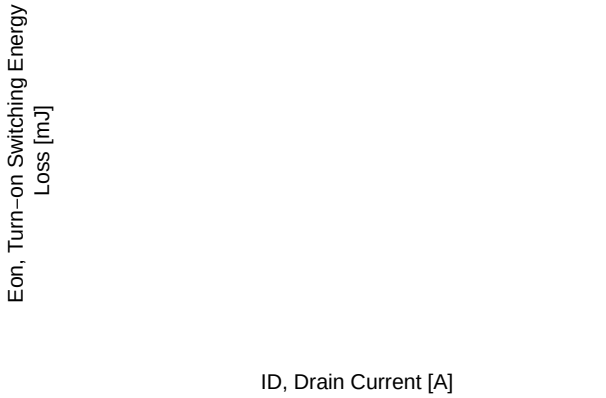


Figure 16. Typ. Turn−on Switching Energy Loss

Figure 17. Typ. Turn−off Switching Energy Loss

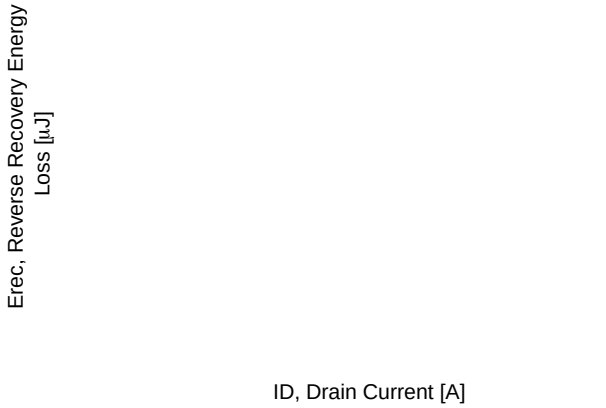


Figure 18. Typ. Reverse Recovery Energy Loss

TURN−ON/OFF SWITCHING WAVEFORM

Switching Condition: VPN = 600 V, VDD = 18 V, Tj = 25°C, Id = 40 A.

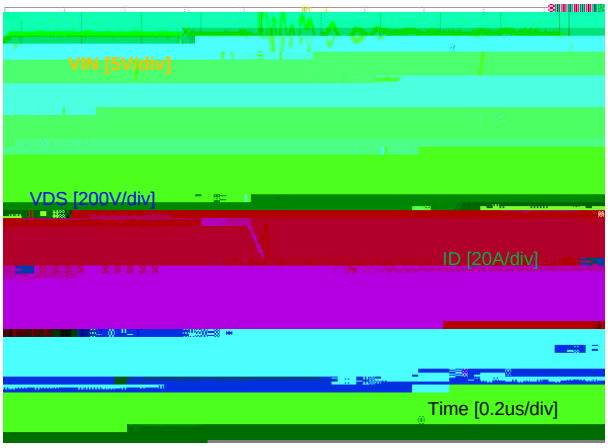


Figure 25. Turn−on Switching Waveform

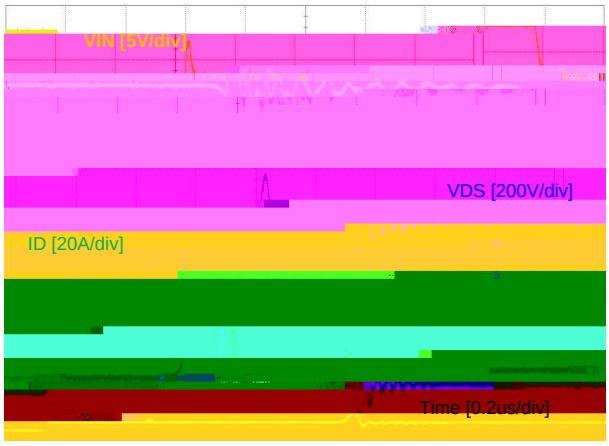


Figure 26. Turn−off Switching Waveform

Switching Condition: VPN = 600 V, VDD = 18 V, Tj = 150°C, Id = 40 A.

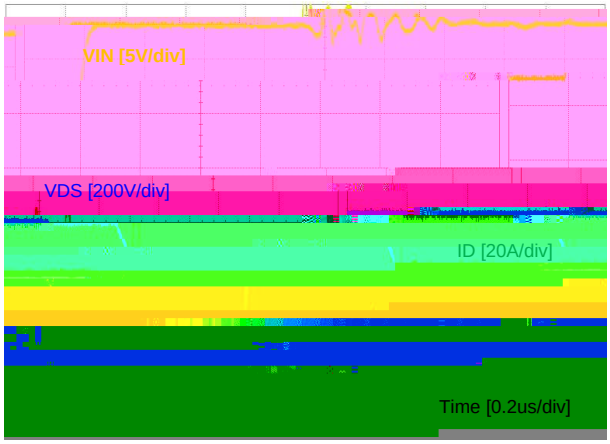


Figure 27. Turn−on Switching Waveform

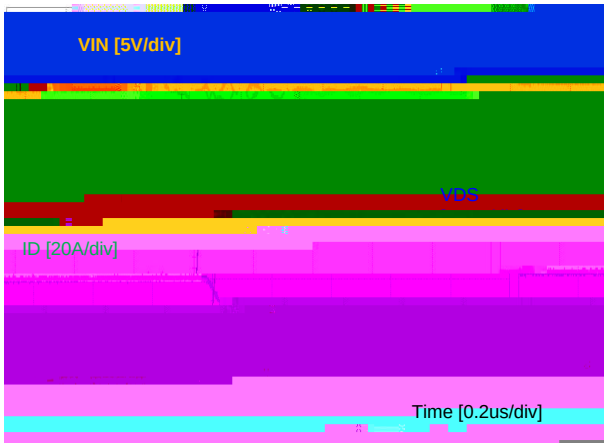
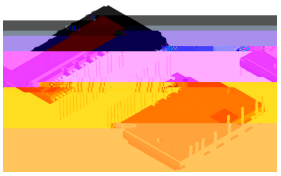
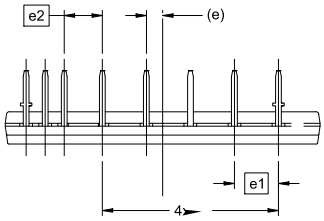


Figure 28. Turn−off Switching Waveform

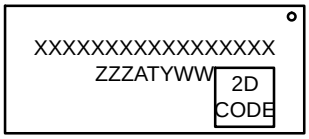


DIP39, 54.50x31.00x5.60, 1.78P
CASE MODGC
ISSUE B

DATE 21 DEC 2023



GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
ZZZ = Assembly Lot Code
AT = Assembly & Test Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.