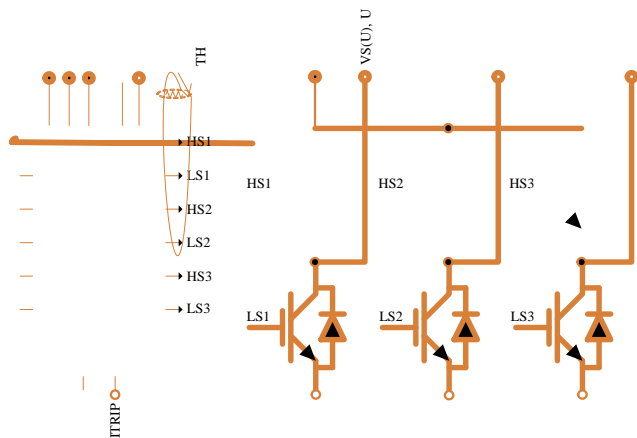


Intelligent Power Module (IPM) 600 V, 10 A

NFAP1060L3TT

The NFAP1060L3TT is a fully-integrated inverter power stage consisting of a high-voltage driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless-DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm. The power stage has a full range of protection functions including cross-



NFAP1060L3TT

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VPN

P:13

NU:17

NV:19

HIN(U):20

HIN(V):22

NW:21

HIN(W):23

LIN(U):24

LIN(V):25

LIN(W):26

VS(U), U:10

FLTEN:18

VS(V), V:6

TH:27

VDD:28

VS(W), W:2

VSS:29

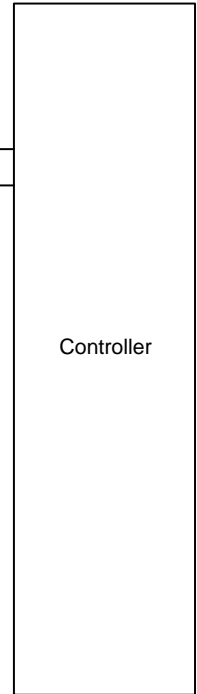


Figure 2. Application Schematic

NFAP1060L3TT

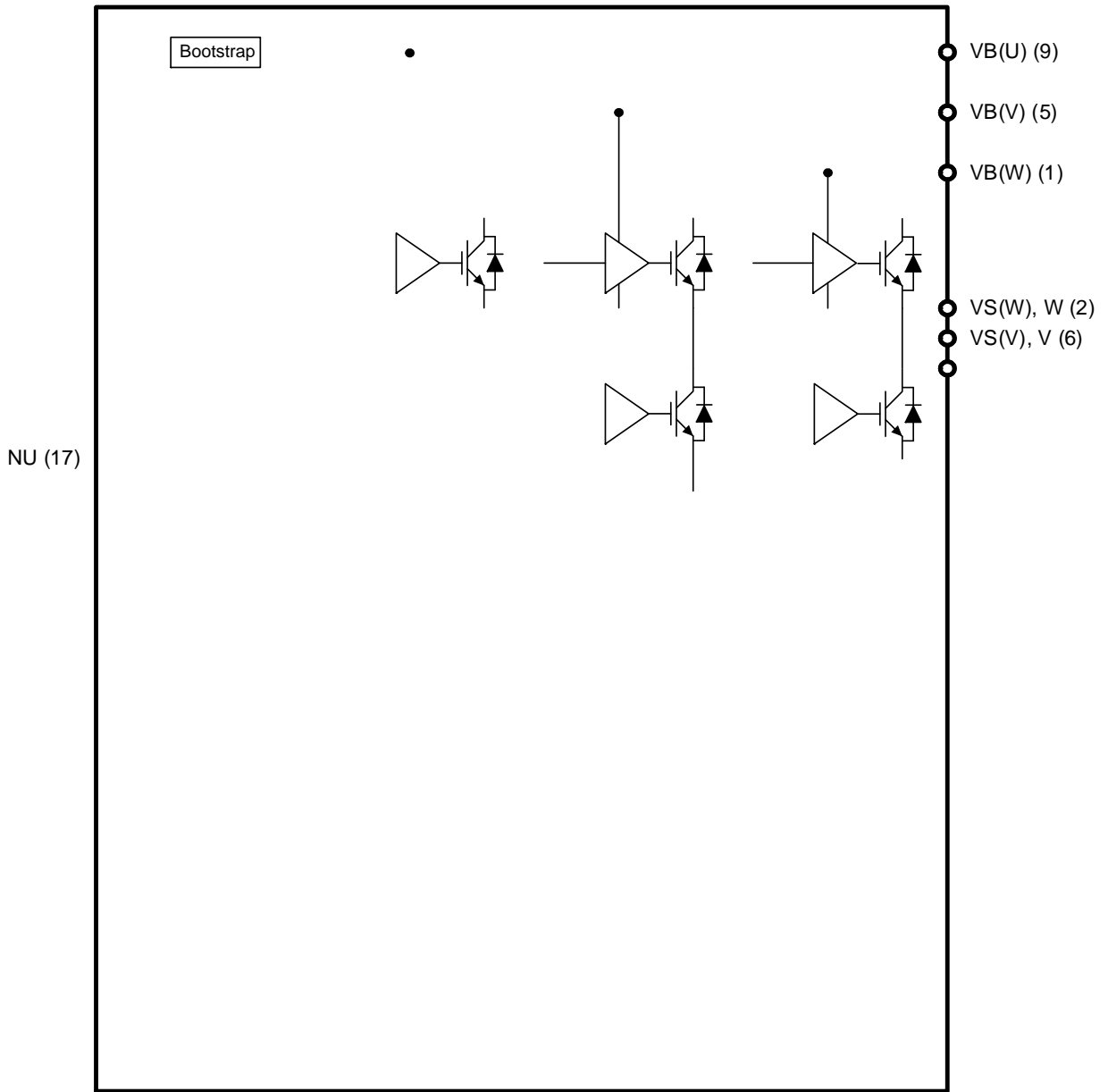


Figure 3. Simplified Block Diagram

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Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1		

NFAP1060L3TT

Table 3. RECOMMENDED OPERATING RANGES

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	VPN	P-NU,NV,NW	0	280	450	V
High-Side Control Bias voltage	VBS	VB(U)-VS(U), VB(V)-VS(V), VB(W)-VS(W)	13.0	15	17.5	V
Control Supply Voltage	VDD	VDD-VSS	14.0	15	16.5	V
ON-state Input Voltage	VIN(ON)					

NFAP1060L3TT



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TYPICAL CHARACTERISTICS INV SECTION

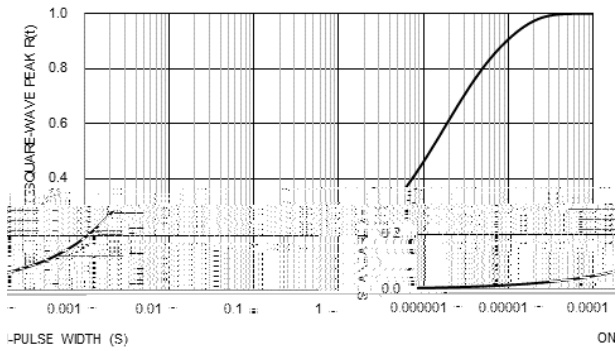


Figure 8. Thermal Impedance Plot

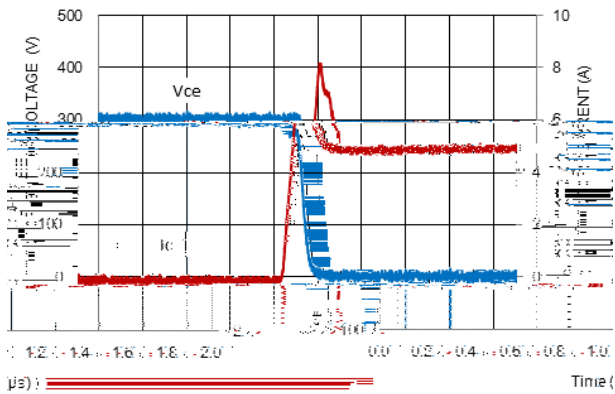


Figure 9. Turn-on Waveform
 $T_j = 100^\circ\text{C}$, $V_{CC} = 300\text{ V}$

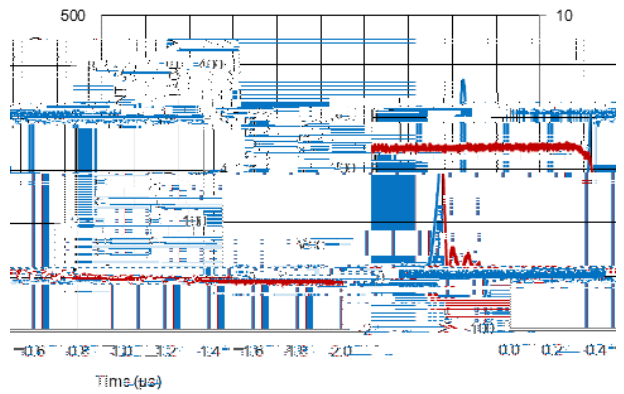
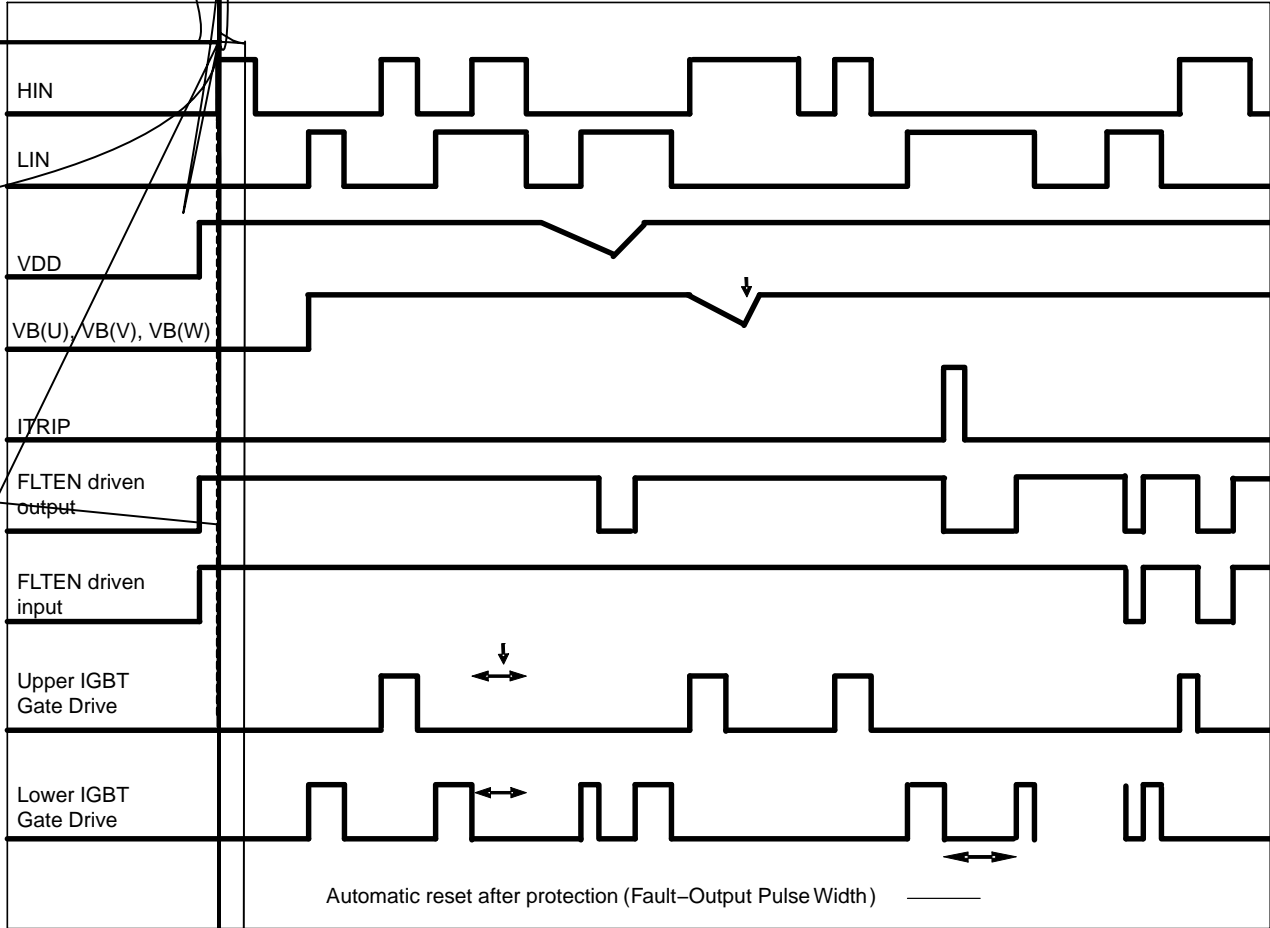


Figure 10. Turn-off Waveform
 $T_j = 100^\circ\text{C}$, $V_{CC} = 300\text{ V}$

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APPLICATIONS INFORMATION



NFAP1060L3TT

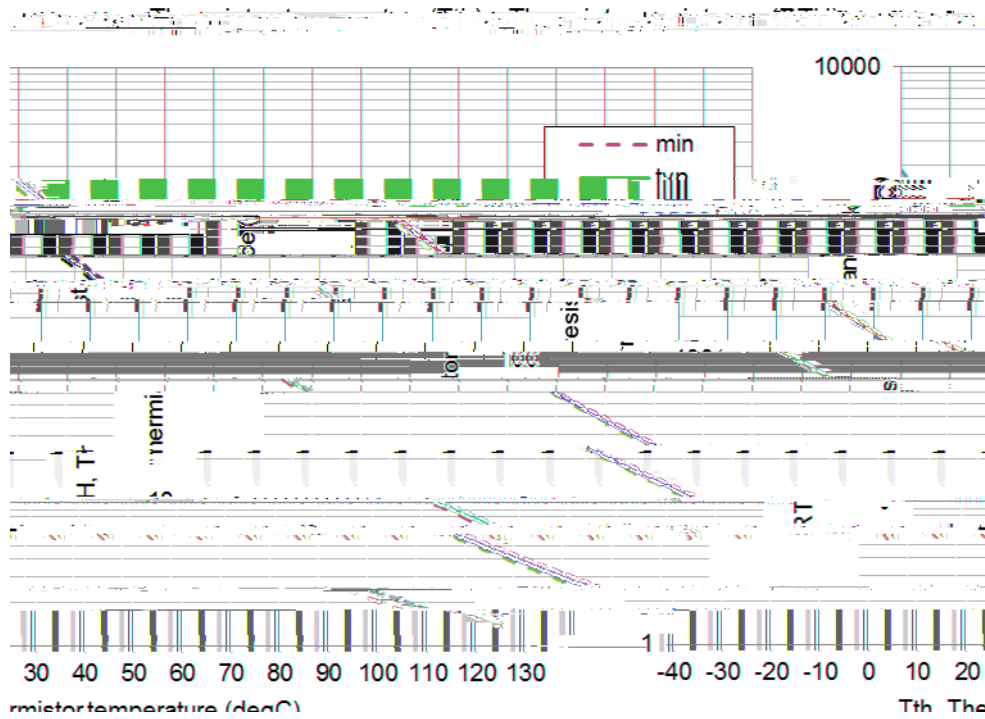


Figure 12. Thermistor Resistance vs. Thermistor Temperature

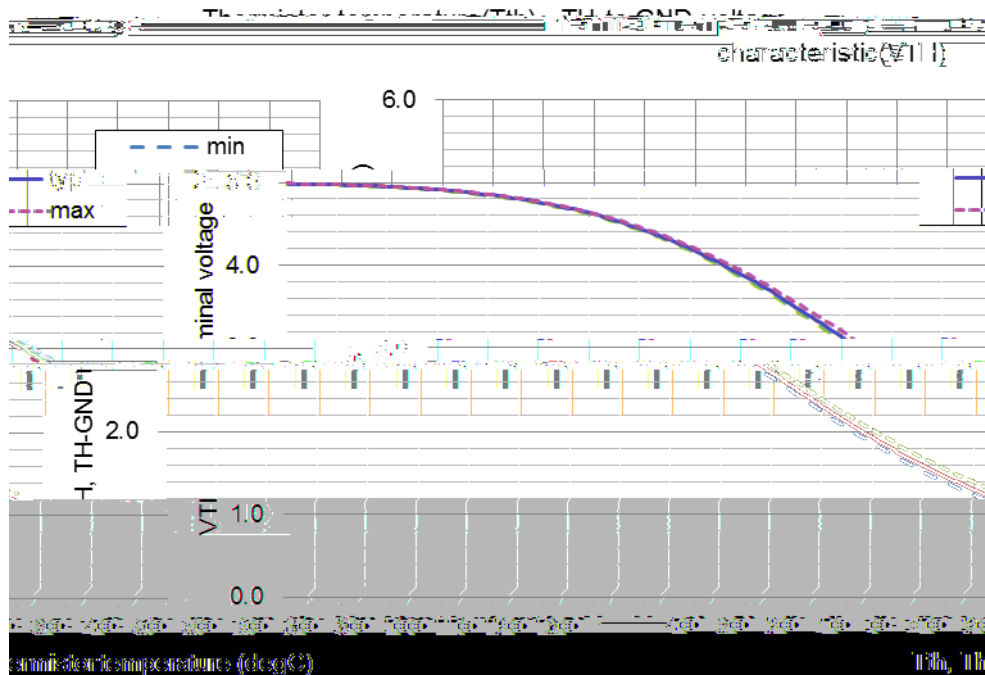


Figure 13. Thermistor Voltage vs. Thermistor Temperature
 Conditions: $R_{TH} = 4.7 \text{ k}\Omega$, pull-up voltage 5.0 V (see Figure 12)

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FLTEN Pin

The FLTEN pin is connected to an open–drain FAULT

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TEST CIRCUITS

I_{ces}, I_R(DB)

	U+	V+	W+	U-	V-	W-
A	13	13	13	10	6	2
B	10	6	2	17	19	21

U+,V+,W+ : High side phase
U-,V-,W- : Low side phase

	U(DB)	V(DB)	W(DB)
A	9	5	1
B	29	29	29

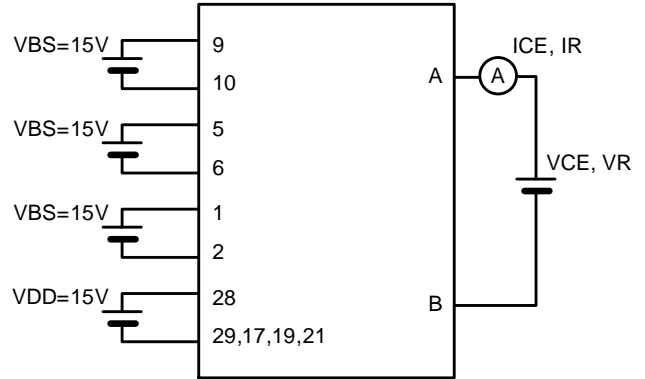


Figure 15. Test Circuit for I_{CE}

V_{CE(sat)} (Test by pulse)

U+	V+	W+	U-	V-	W-
13	13	13	10	6	2
10	6	2	17	19	21
20	22	23	24	25	26

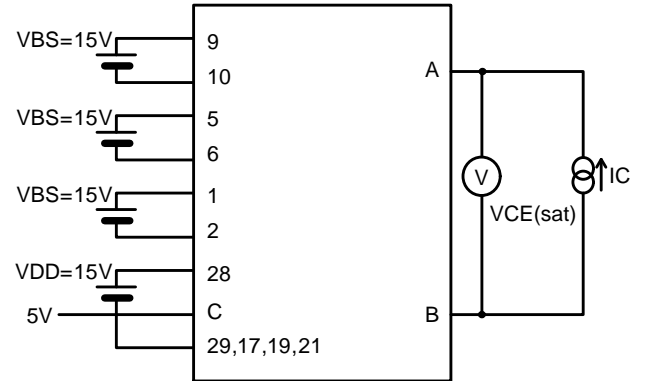


Figure 16. Test Circuit for V_{CE(SAT)}

else)

U+	V+	W+	U-	V-	W-
13	13	13	10	6	2
10	6	2	17	19	21

U(DB)	V(DB)	W(DB)
9	5	1
28	28	28

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SWITCHING TIME (The circuit is a representative example of the lower side U phase.)

	U+	V+	W+	U-	V-	W-
A	13	13	13	13	13	13
B	17	19	21	17	19	21
C	10	6	2	13	13	13

D

SIP29 44.00x20.90x5.50, 1.27P
CASE 127FB
ISSUE B

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