

Device

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Typical Applications

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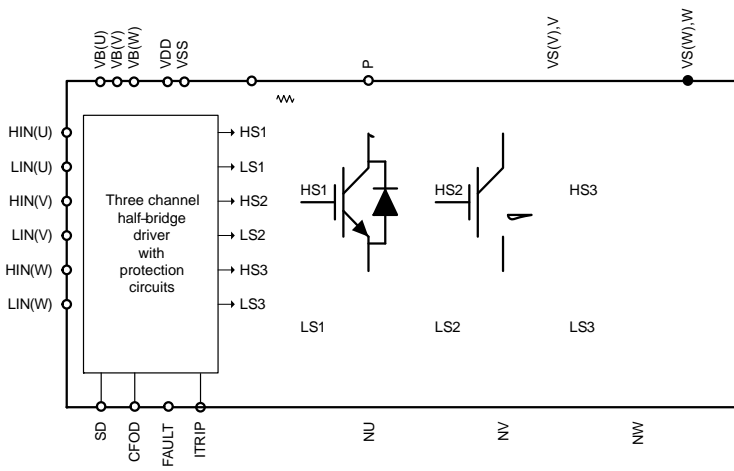


Figure 1. Function Diagram



NFAQ0860L33T

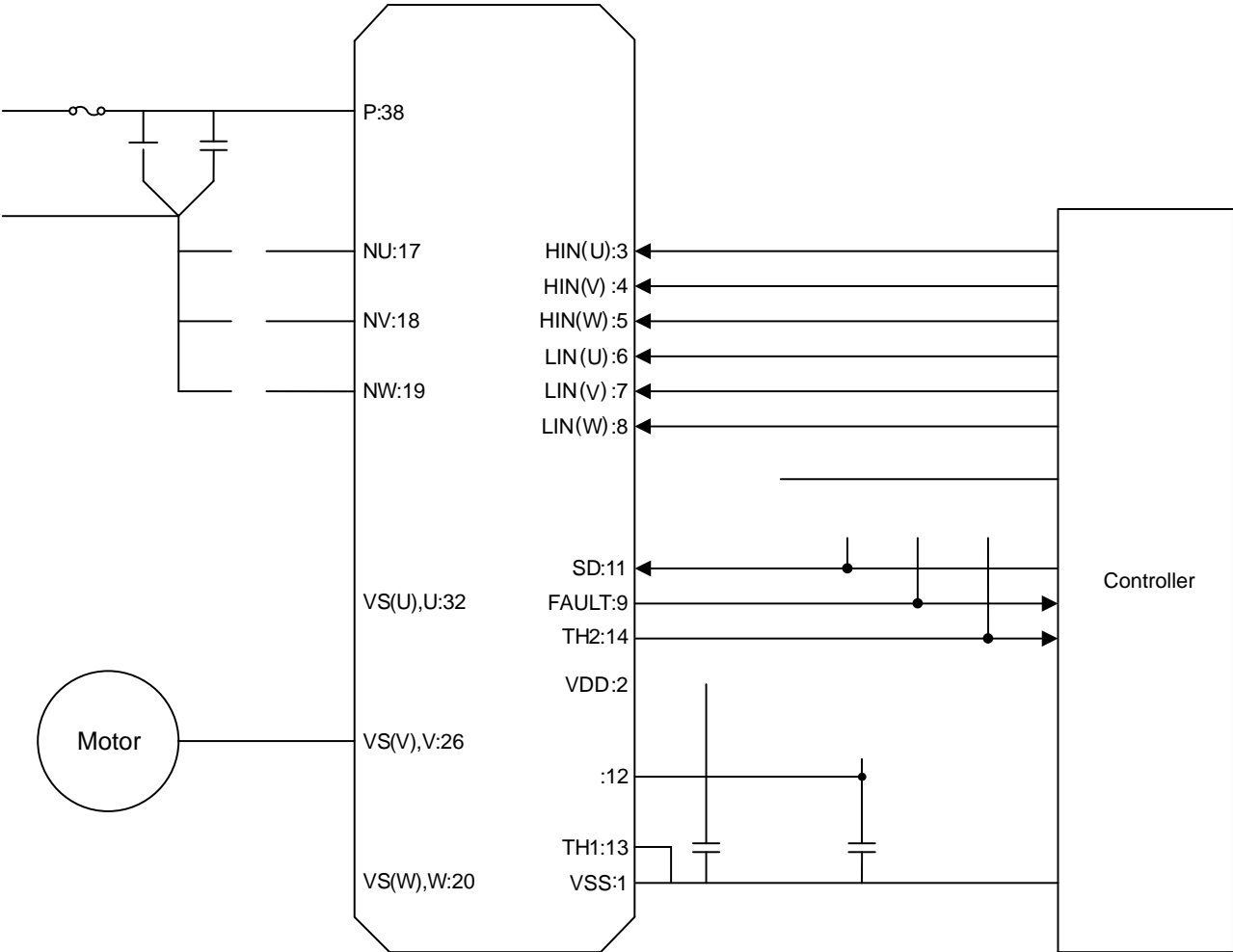


Figure 2. Application Schematic

# NFAQ0860L33T

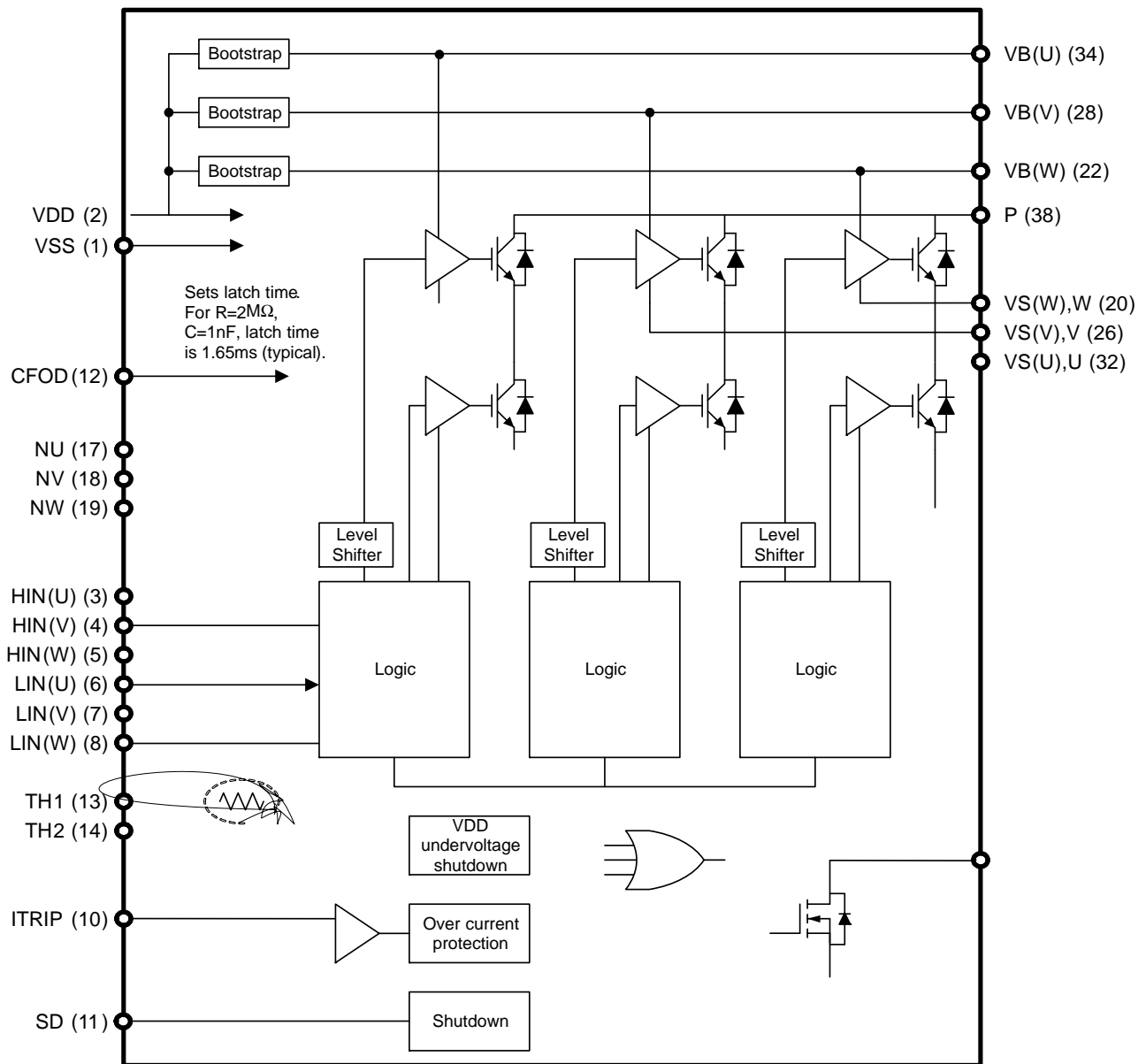


Figure 3. Simplified Block Diagram

# NFAQ0860L33T

**Table 1. PIN FUNCTION DESCRIPTION**

<b>Pin</b>	<b>Name</b>	<b>Description</b>
1	VSS	Low-Side Common Supply Ground
2	VDD	Low-Side Bias Voltage for IC and IGBTs Driving
3	HIN(U)	Signal Input for High-Side U Phase
4	HIN(V)	Signal Input for High-Side V Phase

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**Table 2. ABSOLUTE MAXIMUM RATINGS** at  $T_C = 25^\circ\text{C}$  (Note 1)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	VPN	P-NU,NV,NW, VPN (surge) < 500 V (Note 2)	450	V
Collector – Emitter Voltage	VCES	P-U,V,W; U-NU; V-NV; W-NW	600	V
Each IGBT Collector Current	IC	P,U,V,W,NU,NV,NW terminal current	±8	A
		P,U,V,W,NU,NV,NW terminal current, $T_c = 100^\circ\text{C}$	±4	A
Each IGBT Collector Current (Peak)	ICp	$T_c = 25^\circ\text{C}$ , Under 1 ms Pulse Width	±16	A
Corrector Dissipation	Pc	$T_c = 25^\circ\text{C}$ , Per One Chip	32	W
High-Side Control Bias voltage	VBS	VB(U)-VS(U), VB(V)-VS(V), VB(W)-VS(W) (Note 3)	-0.3 to +20.0	V
Control Supply Voltage	VDD	VDD-VSS	-0.3 to +20.0	V
Input Signal Voltage	VIN	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) – VSS	-0.3 to $V_{DD}$	V
FAULT Terminal Voltage	VFAULT	FAULT-VSS	-0.3 to $V_{DD}$	V
CFOD Terminal Voltage	VCFOD	CFOD-VSS	-0.3 to $V_{DD}$	V
Current Sensing Input Voltage	VITRIP	ITRIP-VSS	-0.3 to +10.0	V

6000 .68036 14.4 Tf.5797 0 TD-SFe448.044 502.243 .68033 14.4 ref4 0 0 8 264.10VCFOD

# NFAQ0860L33T

**Table 4. ELECTRICAL CHARACTERISTICS** at  $T_C = 25\text{ }^\circ\text{C}$ ,  $V_{BIAS}$  (VBS, VDD) = 15 V unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
<b>Power Output Section</b>						
Collector–Emitter Leakage Current	$V_{CE} = 600\text{ V}$	ICES	–	–	100	$\mu\text{A}$
Collector–Emitter Saturation Voltage	$I_N = 5\text{ V}$ , $I_C = 8\text{ A}$ , $T_j = 25\text{ }^\circ\text{C}$	VCE(sat)	–	2.4	3.0	V
	$I_N = 5\text{ V}$ , $I_C = 4\text{ A}$ , $T_j = 100\text{ }^\circ\text{C}$		–	1.9	–	V
FWDi Forward Voltage	$I_N = 0\text{ V}$ , $I_C = -8\text{ A}$ , $T_j = 25\text{ }^\circ\text{C}$	VF	–	2.1	2.7	V
	$I_N = 0\text{ V}$ , $I_C = -4\text{ A}$ , $T_j = 100\text{ }^\circ\text{C}$		–	1.6	–	V
Junction to Case Thermal Resistance	Inverter IGBT Part (per 1/6 Module)	Rth(j–c)Q	–	–	3.9	$^\circ\text{C/W}$
	Inverter FRD Part (per 1/6 Module)	Rth(j–c)F	–	–	<b>733</b>	$^\circ\text{C/W}$
<b>Switching Character</b>						
Switching Time	IC = 8 A, VPV = 300 V, Tj = 25°C, Inductive Switching	tON	–	0.4	1.1	$\mu\text{s}$
		tOFF	–	0.4	1.1	$\mu\text{s}$
Turn–on Switching Loss	IC = 8 A, VPV = 300 V, Tj = 25°C	EON	–	190	–	$\mu\text{J}$
Turn–off Switching Loss		E <sub>OFF</sub>	–	90	–	$\mu\text{J}$
Total Switching Loss		OFF	–	–	–	–



**APPLICATIONS INFORMATION**

**Input / Output Timing Chart**

NOTES:

1. This section of the timing diagram shows the effect of cross-conduction prevention.

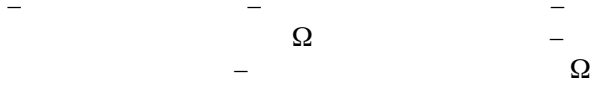
**Figure 12. Input / Output Timing Chart**





# NFAQ0860L33T

## FAULT Pin



## Under-voltage Protection



# NFAQ0860L33T

## TEST CIRCUITS

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	U+	V+	W+	U-	V-	W-
A	38	38	38	32	26	20

•

	U+	V+	W+
A	2	2	2
B	34	28	22
C	6	7	8

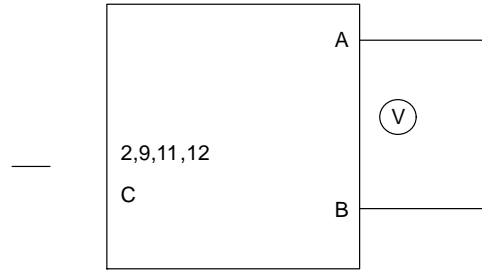
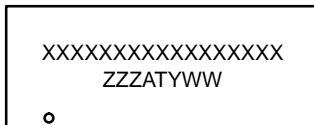


Figure 19. Test Circuit for RB

**DIP38, 29.60x18.20x9.80, 1.00P (EP-3)**  
CASE 125BT  
ISSUE B

DATE 26 APR 2023

**GENERIC  
MARKING DIAGRAM\***



XXXX = Specific Device Code  
ZZZ = Lot ID  
AT = Assembly & Test Location  
Y = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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