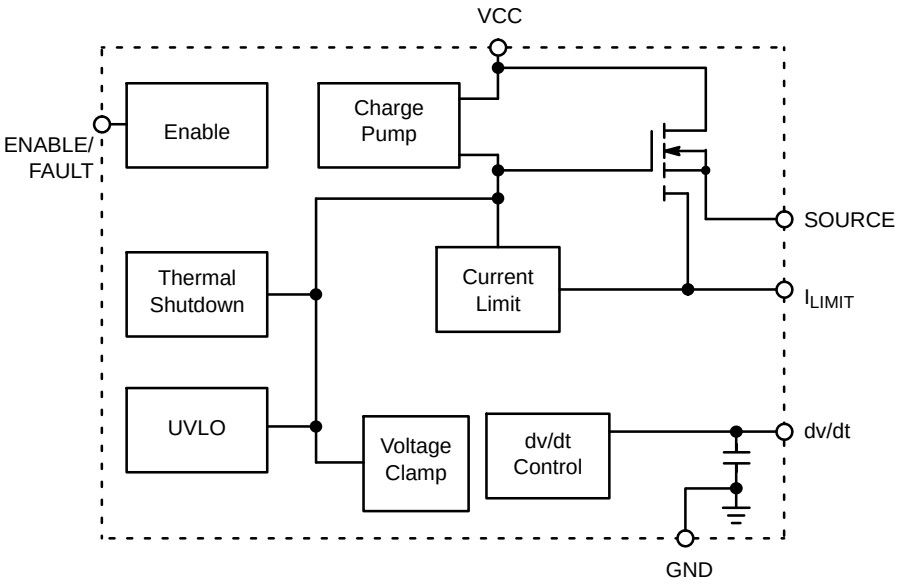
+5 . E F

5135

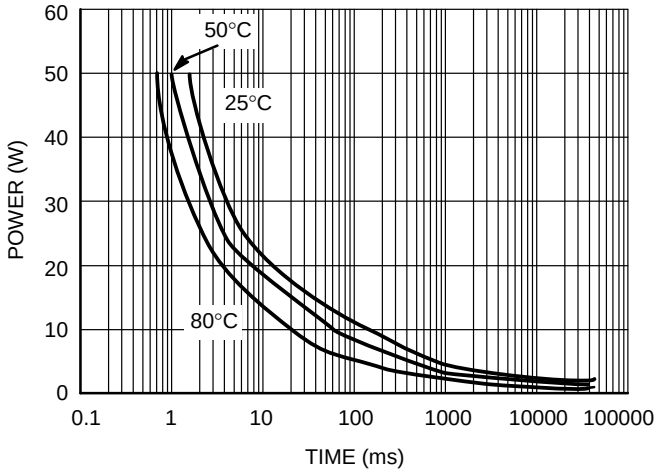
The NIS5135 is a cost effective, resettable fuse which can greatly enhance the reliability of a hard drive or other circuit from both

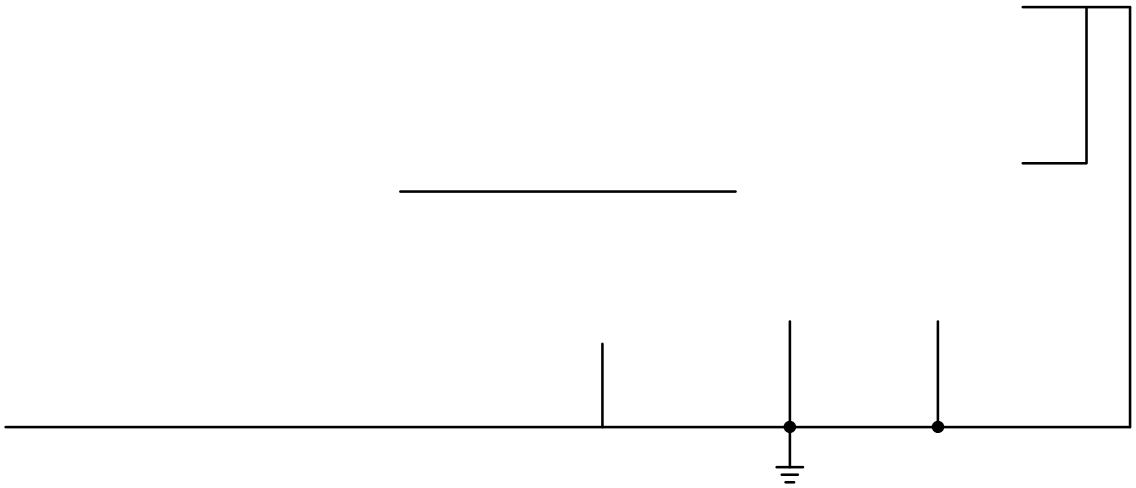
Publication Order Number:

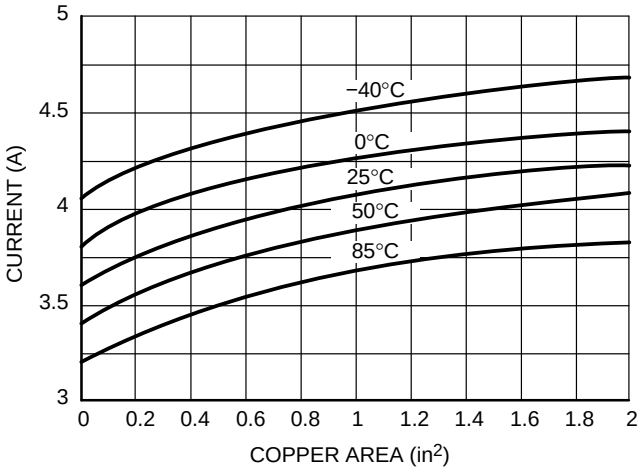


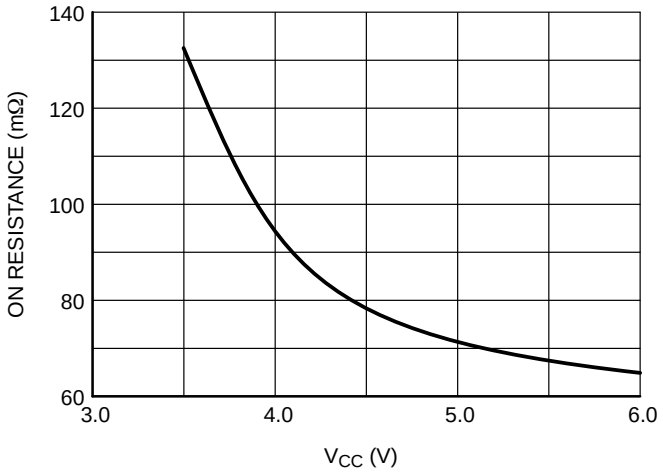
1−5	Source	This pin is the source of the internal power FET and the output terminal of the fuse.
7	I_{Limit}	A resistor between this pin and the source pin sets the overload and short circuit current limit levels.
8	Enable/Fault	The enable/fault pin is a tri−state, bidirectional interface. It can be used to enable or disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. It can also be connected to another device in this family to cause a simultaneous shutdown during thermal events.
9	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over a period of 2 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
10	Ground	Negative input voltage to the device. This is used as the internal reference for the IC.
11 (belly pad)	V_{CC}	Positive input voltage to the device.

(Unless otherwise noted: V_{CC} = 5.0 V, C_L = 70 μ


60
50
40
30
20
10
0
POWER (W)
50°C
25°C
80°C
0.1
1
10
100
1000
10000
100000
TIME (ms)




5
4.5
4
3.5
3
CURRENT (A)
−40°C
0°C
25°C
50°C
85°C
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
COPPER AREA (in2)



This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The dv/dt of the output voltage will be controlled by the internal dv/dt circuit. The output voltage will slew from 0 V to the rated output voltage in 2 ms, unless additional capacitance is added to the dv/dt pin.

The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip. The current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage to 6.65 V in the event that the input exceeds that level.

An internal charge pump provides bias for the gate voltage of the internal n−channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (V_{CC}) and ground.

The current limit circuit uses a SENSEFET along with a reference and amplifier to control the peak current in the device. The SENSEFET allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor as well as increasing the value and decreasing the power rating of the sense resistor. Sense resistors are typically in the tens of ohms range with power ratings of several milliwatts making them very inexpensive chip resistors.

The current limit circuit has two limiting values, one for overload events which are defined as the mode of operation in which the gate is high and the FET is fully enhanced. The short circuit mode of operation occurs when the device is actively limiting the current and the gate is at an intermediate level. For a more detailed description of this circuit please refer to application note AND8140.

There are two methods of biasing the current limit circuit for this device. They are shown in the two application figures. Direct current sensing connects the sense resistor between the current limit pin and the load. This method includes the bond wire resistance in the current limit circuit. This resistance has an impact on the current limit levels for a given resistor and may vary slightly depending on the impedance between the sense resistor and the source pins. The on resistance of the device will be slightly lower in this configuration since all five source pins are connected in parallel and therefore, the effective bond wire resistance is one fifth of the resistance for any given pin.

The other method is Kelvin sensing. This method uses one of the source pins as the connection for the current sense resistor. This connection senses the voltage on the die and therefore any bond wire resistance and external impedance on the board have no effect on the current limit levels. In this configuration the on resistance is slightly increased relative to the direct sense method since only for of the source pins are used for power.

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds 6.65 V, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level, the output switch will be switched to a high impedance state.

The dv/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor.

The default ramp time is approximately 2 ms. This can be modified by adding an external capacitor at the dv/dt pin. This pin includes an internal current source of approximately 85 nA. Since the current level is very low, it is important to use a ceramic cap or other low leakage capacitor. Aluminum electrolytic capacitors are not recommended for this circuit.

The ramp time from 0 to the nominal output voltage can be determined by the following equation, where *t* is in seconds:

$$t_{0-5} = 30e6 \cdot (50\ pF + C_{ext})$$

$$C_{ext} = \frac{t_{0-5}}{30e6} - 50\ pF$$

Where:
C is in Farads
t is in Seconds

Any time that the unit shuts down due to a fault, enable shut−down, or recycling of input power, the timing capacitor will be discharged and the output voltage will ramp from 0 at turn on.

The Enable/Fault Pin is a multi−function, bidirectional pin that can control the output of the chip as well as send information to other devices regarding the state of the chip. When this pin is low, the output of the fuse will be turned off. When this pin is high the output of the fuse will be turned−on. If a thermal fault occurs, this pin will be pulled low to an intermediate level by an internal circuit.

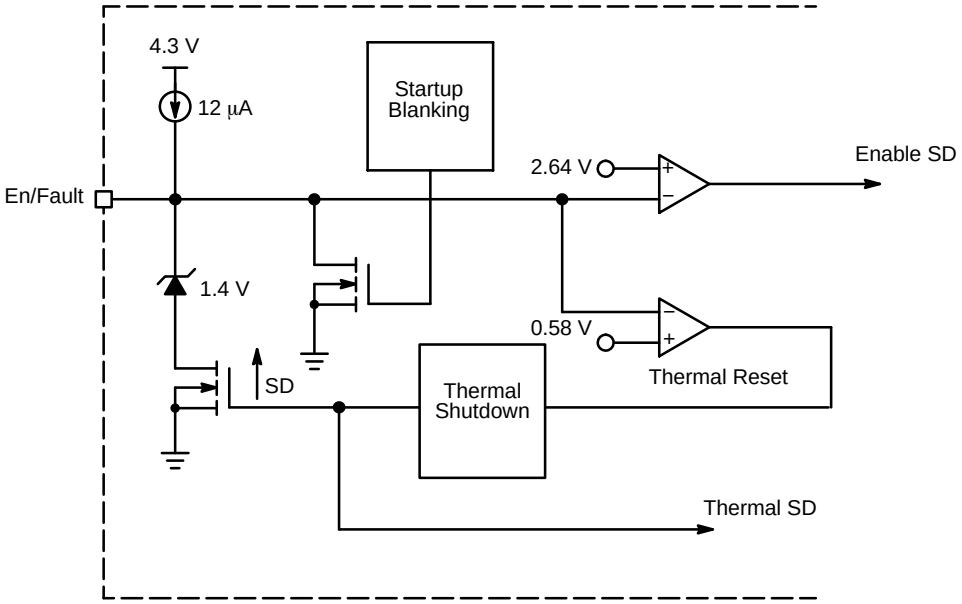
To use as a simple enable pin, an open drain or open collector device should be connected to this pin. Due to its tri−state operation, it should not be connected to any type of logic with an internal pullup device.

If the chip shuts down due to the die temperature reaching its thermal limit, this pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred. If this pin is tied to another device in this family (NIS5132 or NIS5135), a thermal shutdown of one device will cause both devices to disable their outputs. Both devices will turn on once the fault is removed for the auto−retry devices.

For the latching thermal device, the outputs will be enabled after the enable pin has been pulled to ground with an external switch and then allowed to go high or after the input power has been recycled. For the auto retry devices, both devices will restart as soon as the die temperature of the device in shutdown has been reduced to the lower thermal limit. The thermal options are listed in the ordering table.

The NIS5135 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. Output power can be restored by either recycling the input power or toggling the enable pin. Power will automatically be reapplied to the load for auto−retry devices once the die temperature has been reduced by 45°C.

The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 150°C for extended periodt volte01 for a[illegible]not recommended to operate this devic



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NIS5135MN1TXG (Note 8)	Thermal Latching	DFN10 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 8)
NIS5135MN2TXG (Note 8)	Thermal Auto−Retry	DFN10 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 8)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. Products processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.