+12 Volt Electronic Fuse
NIS5232 Series

The NIS5232 is a cost effective, resettable fuse which can greatly enhance the reliability of a hard drive or other circuit from both catastrophic and shutdown failures.

It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits. It also includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue operation.

DFN10
CASE 485C

MARKING DIAGRAM

Features

- Integrated Power Device
- Power Device Thermally Protected
- No External Current Shunt Required
- 9 V to 18 V Input Range
- 44 mΩ Typical
- Internal Charge Pump
- Internal Undervoltage Lockout Circuit
- Internal Overvoltage Clamp
- ESD Ratings: Human Body Model (HBM); 1500 V
  Machine Model (MM); 200 V
- UL2367 Approved (UL File #E466553)
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Hard Drives
- Mother Board Power Management

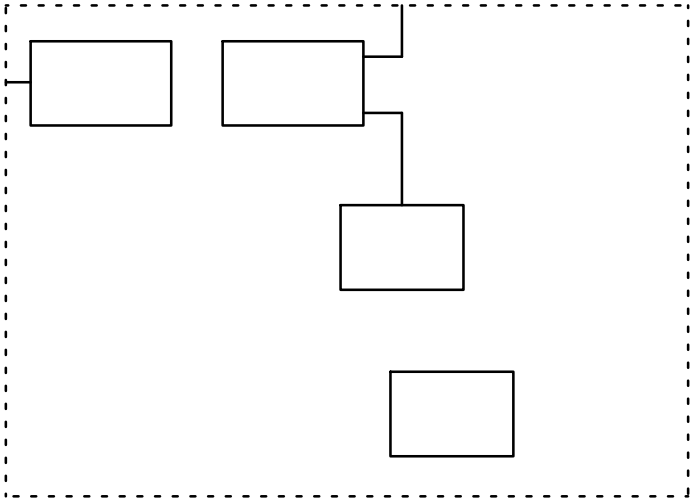

Figure 1. Block Diagram

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 12 V, C_L = 100 μF, dv/dt pin open, R_{LIMIT} = 10 Ω, T_j = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
Delay Time (enabling of chip to I_D = 100 mA with 1 A resistive load)	T_{dly}		220		μs
Kelvin ON Resistance (Note 5) T_J = 140°C (Note 6)	R_{DSon}	35	44 62	55	mΩ
Off State Output Voltage (V_{CC} = 18 V_{dc}, V_{GS} = 0 V_{dc}, R_L = □)	V_{off}		190	300	mV
Output Capacitance (V_{DS} = 12 V_{dc}, V_{GS} = 0 V_{dc}, f = 1 MHz)			250		pF
Continuous Current (T_A = 25°C, 0.5 in^2 copper) (Note 6) (T_A = 80°C, minimum copper)	I_D I_D		4.2 2.5		A
THERMAL LATCH					
[redacted]					
Undervoltage Lockout (Turn on, voltage going high)	V_{UVLO}	7.7	8.5	9.3	V
UVLO Hysteresis	V_{Hyst}	–	0.80	–	V
CURRENT LIMIT					
Kelvin Short Circuit Current Limit (R_{Limit} = 15.4 Ω, Note 7)	I_{Lim-SS}	2.75	3.44	4.25	A
Kelvin Overload Current Limit (R_{Limit} = 15.4 Ω, Note 7)	I_{Lim-OL}		4.62		

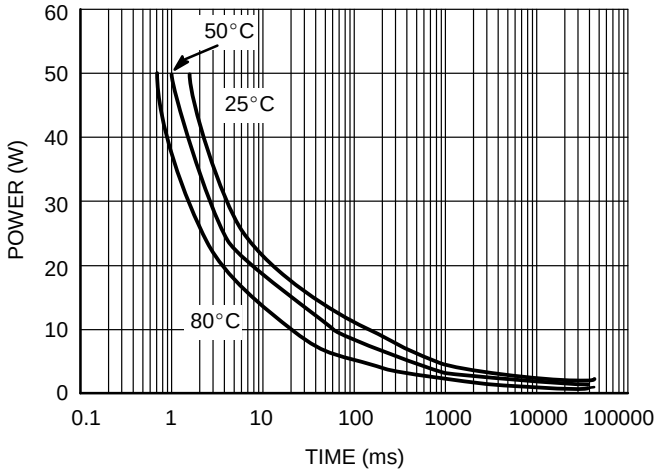

Figure 2. Power Dissipation vs. Thermal Trip Time

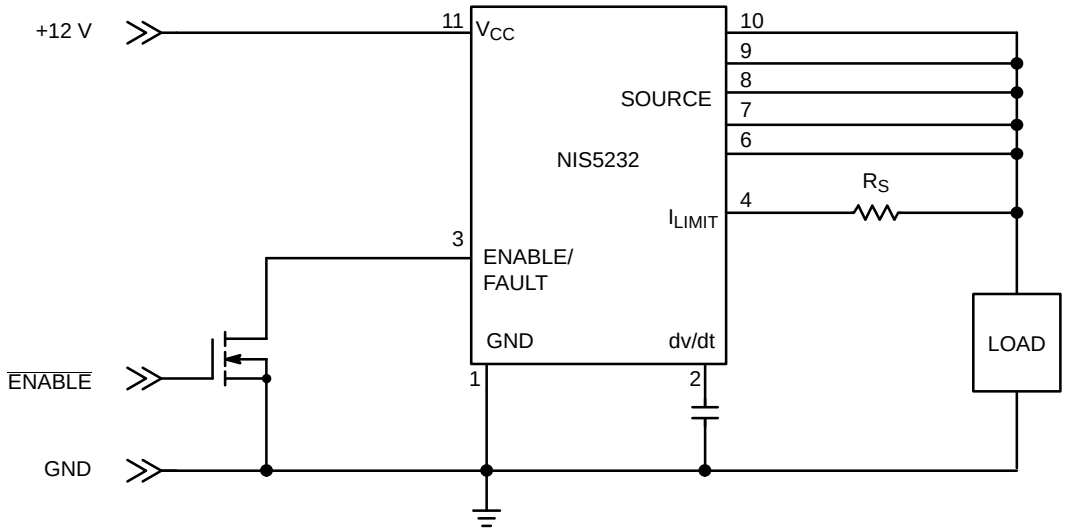

Figure 3. Application Circuit with Direct Current Sensing

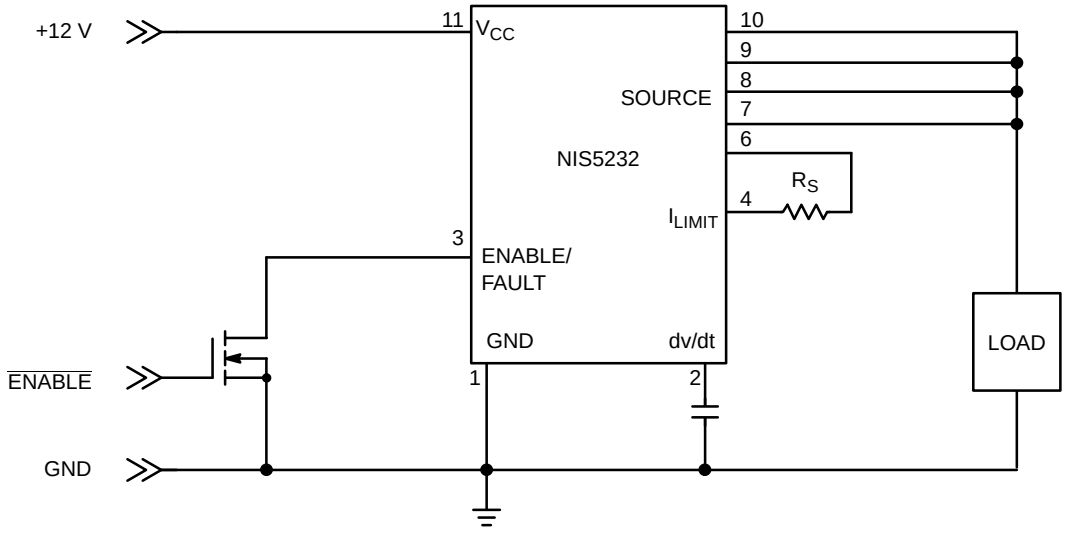

Figure 4. Application Circuit with Kelvin Current Sensing

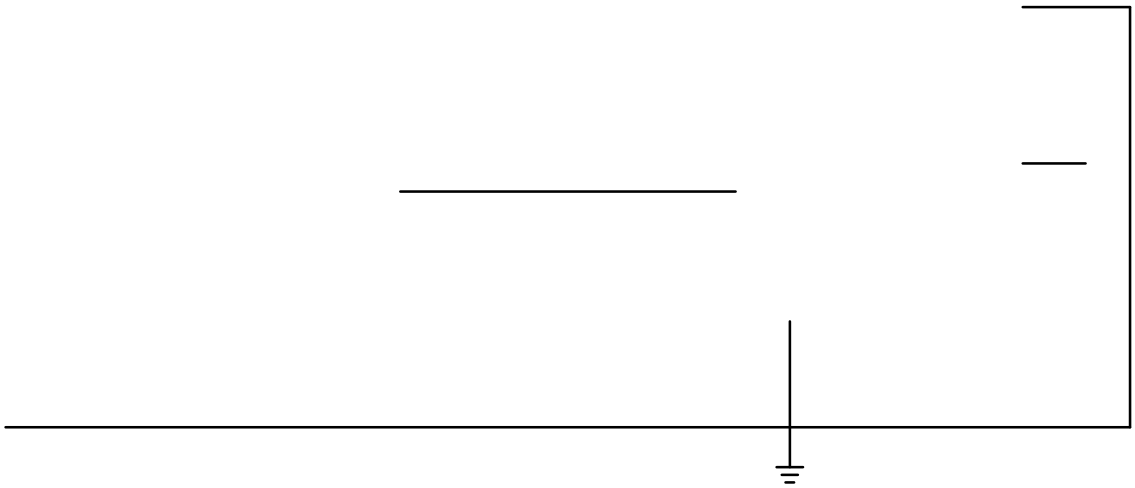

Figure 5. Common Thermal Shutdown

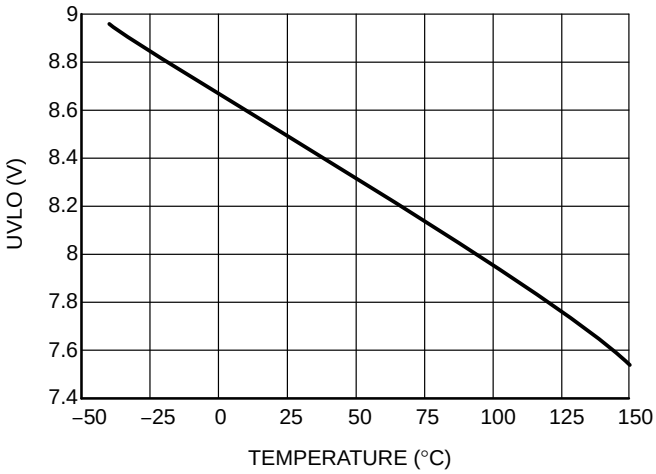

Figure 6. UVLO Turn On

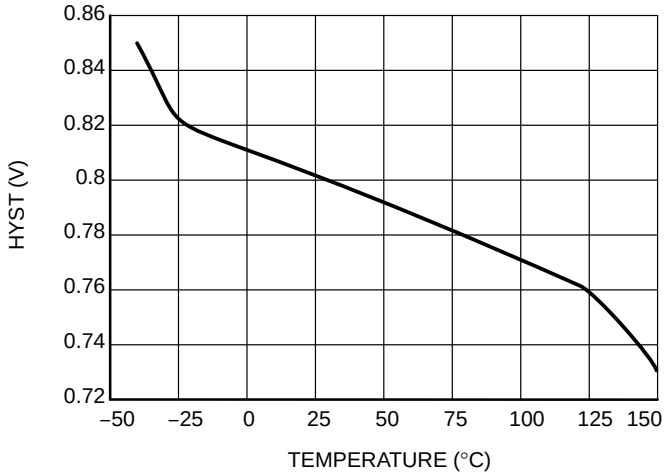

Figure 7. UVLO Hysteresis

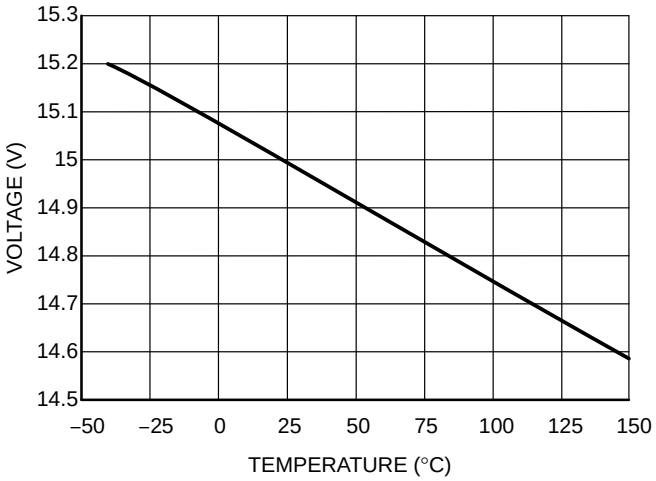

Figure 8. Output Clamping Voltage

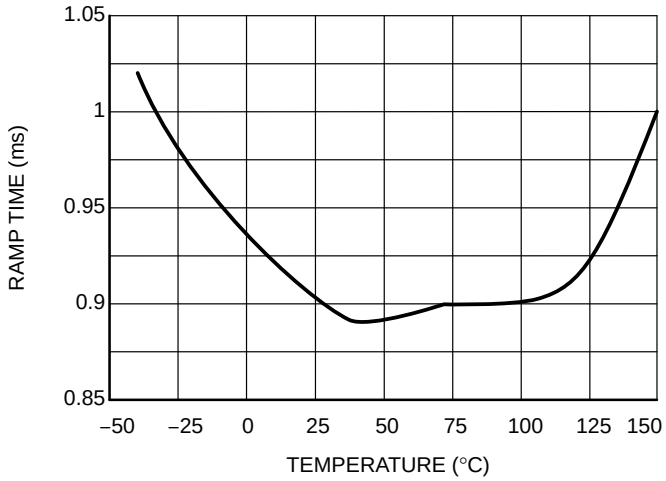

Figure 9. Output Voltage dv/dt Rate

Figure 10. Input Transient Response

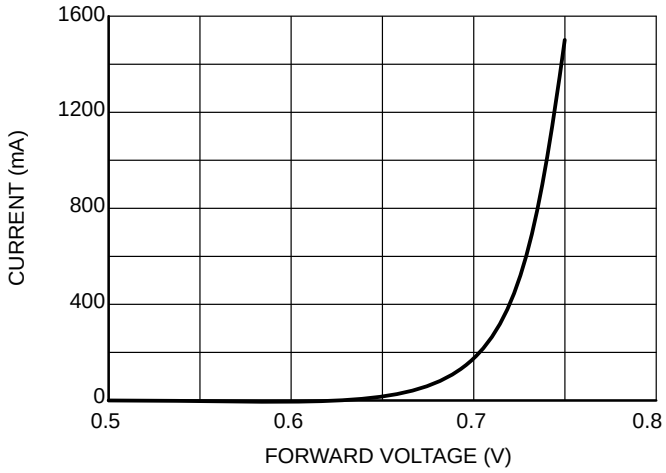

Figure 11. Body Diode Forward Characteristics

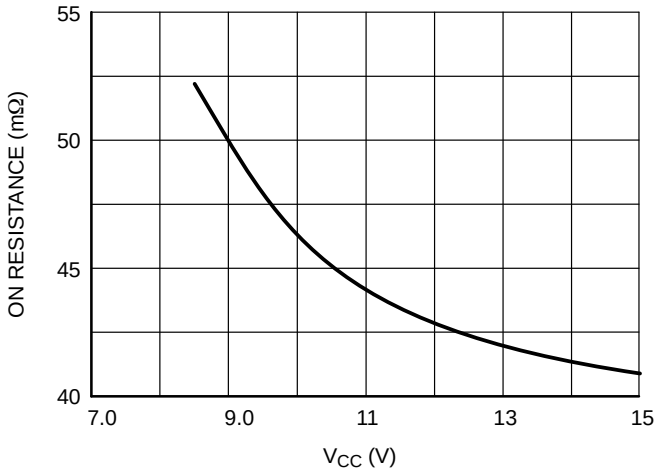

Figure 18. On Resistance vs. V_{CC}

APPLICATION INFORMATION

Basic Operation

This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The dv/dt of the output voltage will be controlled by the internal dv/dt circuit. The output voltage will slew from 0 V to the rated output voltage in 2 ms, unless additional capacitance is added to the dv/dt pin.

The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip. The current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage to 15 V in the event that the input exceeds that level.

An internal charge pump provides bias for the gate voltage of the internal n−channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (V_{CC}) and ground.

Current Limit

The current limit circuit uses a SENSEFET along with a reference and amplifier to control the peak current in the device. The SENSEFET allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor as well as increasing the value and decreasing the power rating of the sense resistor. Sense resistors are typically in the tens of ohms range with power ratings of several milliwatts making them very inexpensive chip resistors.

The current limit circuit has two limiting values, one for short circuit events which are defined as the mode of operation in which the gate is high and the FET is fully enhanced. The overload mode of operation occurs when the device is actively limiting the current and the gate is at an intermediate level. For a more detailed description of this circuit please refer to application note AND8140.

There are two methods of biasing the current limit circuit for this device. They are shown in the two application figures. Direct current sensing connects the sense resistor between the current limit pin and the load. This method includes the bond wire resistance in the current limit circuit. This resistance has an impact on the current limit levels for a given resistor and may vary slightly depending on the impedance between the sense resistor and the source pins. The on resistance of the device will be slightly lower in this configuration since all five source pins are connected in parallel and therefore, the effective bond wire resistance is one fifth of the resistance for any given pin.

The other method is Kelvin sensing. This method uses one of the source pins as the connection for the current sense resistor. This connection senses the voltage on the die and therefore any bond wire resistance and external impedance on the board have no effect on the current limit levels. In this configuration the on resistance is slightly increased relative to the direct sense method since only four of the source pins are used for power.

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds 15 V, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

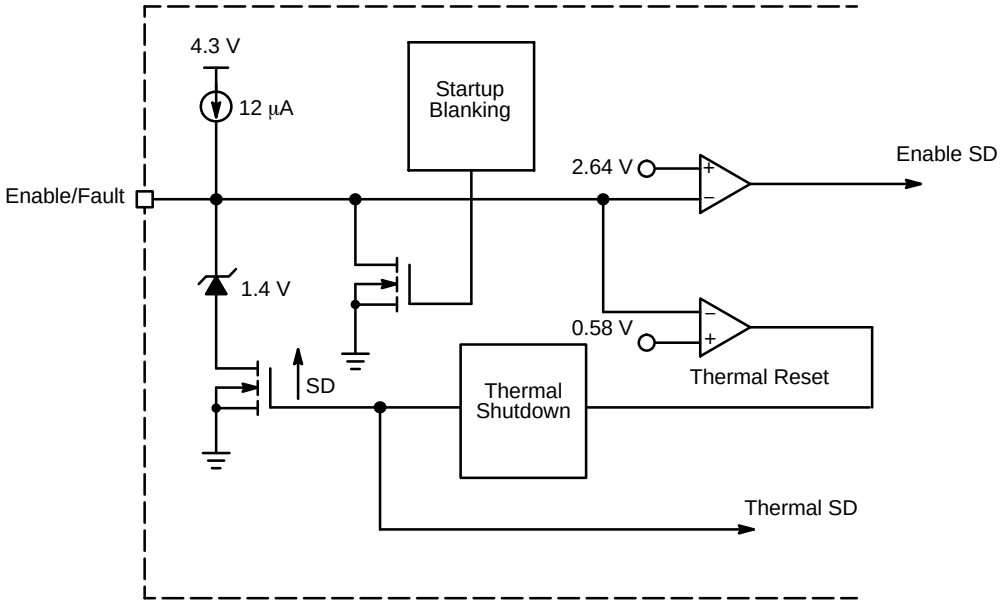

Figure 20. Enable/Fault Simplified Circuit

ORDERING INFORMATION

Device	Features	Package	Shipping†
NIS5232MN1TXG (Note 9)	Thermal Latching	DFN10 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 9)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

9. Products processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.