[illegible] 10, [illegible] 10

The NIS6150 is a cost effective, resettable fuse which can greatly enhance the reliability of a USB application from both catastrophic and shutdown failures.

It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits and to protect the input side circuitry from reverse currents. It includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue its operation.

Features

- 200 mΩ Max $R_{DS(on)}$
- Integrated Reverse Current Protection
- Adjustable Output Current Limit Protection with Thermal Shutdown
- IEC61000 4 2 Level 4 ESD Protection for V_{bus} up to 7 kV
- Fast Response Overvoltage Clamp Circuit with Selectable Level
- Internal Undervoltage Lockout Circuit
- Digital Enable with Separate FLAG for Fault Identification
- Integrated Current Monitoring
- Both Latching and Auto Retry Options Available
- NIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC Q100 Qualified and PPAP Capable
- These Devices are Pb Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Automotive Infotainment
- USB 2.0/3.0/3.1 V_{BUS}
- Solid State Drives
- Mother Boards

WDFNW10, 3 x 3
CASE 515AB

MARKING DIAGRAM

PIN CONNECTIONS

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

Semiconductor Components Industries, LLC, 2018

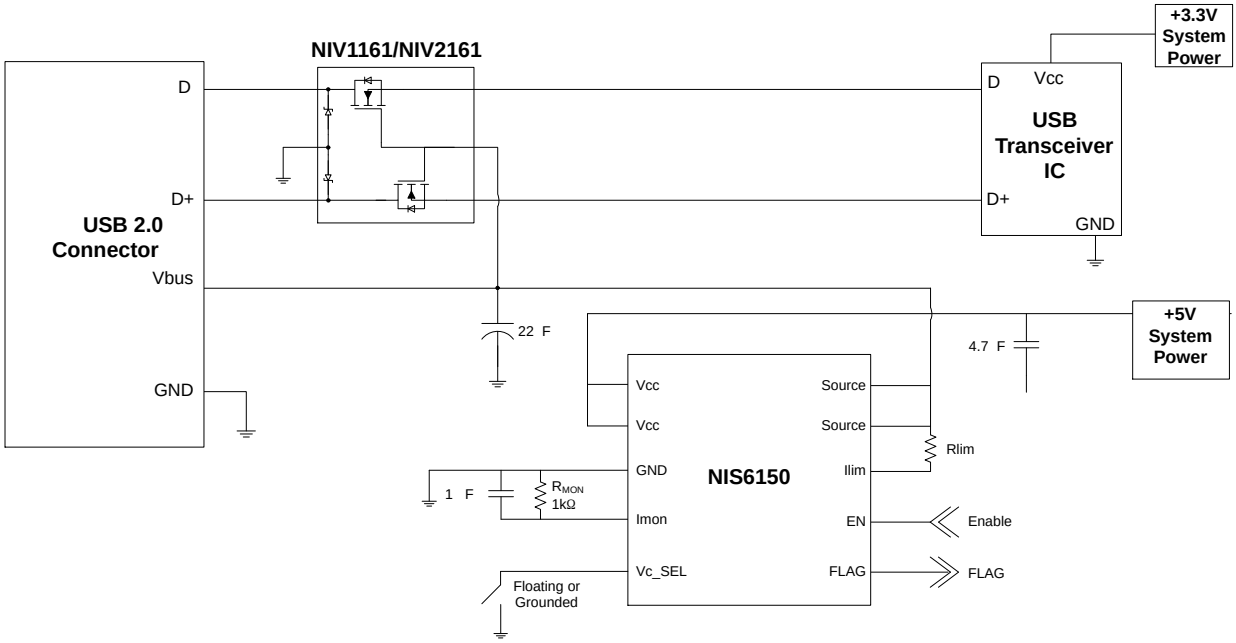


Figure 1. Typical USB 2.0 Application Circuit

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, operating, steady state (V_{CC} to GND) Transient (100 ms)	V_{CC}	0.3 to +10 0.3 to +10	V
Output Voltage, operating, steady state (SRC to GND)	V_{OUT}	0.3 to +20	V
Voltage range on ILIM pin	V_{ILIM}	0.3 to +20	V
Voltage range on Enable pin	V_{EN}	0.3 to 5	V
Voltage range on FLAG pin	V_{FLAG}	0.3 to 6	V
Voltage range on all other pins		0.3 to 5	V
Electrostatic Discharge Human Body Model (All pins) Charged Device Model (All pins) IEC61000 4 2 Contact (Source pins, with 22 μF C_{source} condition)	ESD	 2 1 7	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction to Air (4 layer High K JEDEC JESD51 7 PCB, 100 mm^2, 2 oz. Cu)	θ_{JA}	95	C/W
Thermal Characterization Parameter, Junction to Lead (4 layer High K JEDEC JESD51 7 PCB, 100 mm^2, 2 oz. Cu)	$\psi_{J\ L}$	21	C/W
Thermal Characterization Parameter, Junction to Board (4 layer High K JEDEC JESD51 7 PCB, 100 mm^2, 2 oz. Cu)	$\psi_{J\ B}$	13	C/W
Thermal Characterization Parameter, Junction to Top (4 layer High K JEDEC JESD51 7 PCB, 100 mm^2, 2 oz. Cu)	$\psi_{J\ T}$	20	C/W
Total Continuous Power Dissipation @ T_A = 25 C (4 layer High K JEDEC JESD51 7 PCB, 100 mm^2, 2 oz. Cu) Derate above 25 C	P_{max}	1.3 10.4	W mW/ C
Operating Ambient Temperature Range	T_A	40 to 125	C
Operating Junction Temperature Range	T_J	40 to 150	C
Non operating Temperature Range	T_{STG}	55 to 155	C
Lead Temperature, Soldering (10 Sec)	T_L	260	

ELECTRICAL CHARACTERISTICS

APPLICATIONS INFORMATION

Basic Operation

This device is a self protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The output voltage, which is controlled by an internal dv/dt circuit, will slew from 0 V to the rated output voltage in 1 ms.

The device will remain on as long as the temperature does not exceed the 175 C limit that is programmed into the chip.

The internal current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage in the event that the input exceeds the Vclamp level. This operation can be seen in Figure 5.

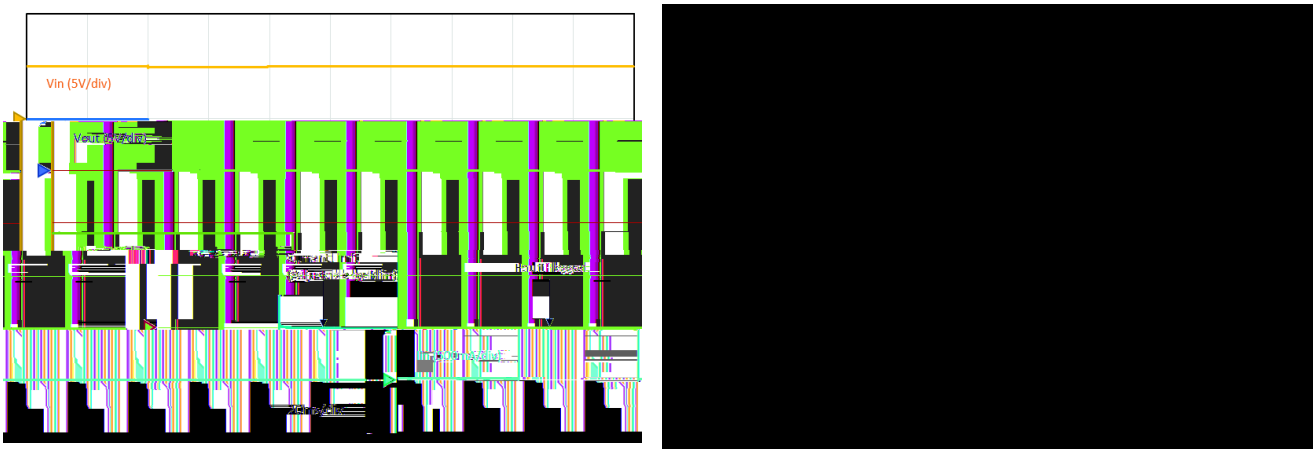
An internal charge pump provides bias for the gate voltage of the internal n channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (VCC) and ground.

The VCC line can generate spike noise in fast transient conditions such as short circuit, and this high peak can cause over stress and malfunction. To prevent this, a low ESR

Latching vs. Auto−Retry

This device features two options regarding its reset ability after a thermal shutdown event. These are called latching and auto retry which are respectively marked MT1 and MT2 as part number suffixes. Upon reaching a thermal shutdown state, a latching device (MT1) will remain shutdown with no power supplied to the output (SRC pins). The only way to reset the device is to either perform a power cycle on the VCC bus or pull the EN pin low (<0.4 V). By doing either of these actions, the fault state is cleared and the device is allowed to pull up the output to its normal, high state.

Instead of remaining in thermal shutdown, an Auto retry device (MT2) will automatically attempt to pull up the output once the die temperature cools to < 135 C. If the fault remains on the output during this attempt, the device will once again enter a short period of current limiting that will eventually lead to thermal shutdown for which the auto retry process will repeat indefinitely.



Latch version | Auto−Retry version

Figure 4. Output Short Circuit

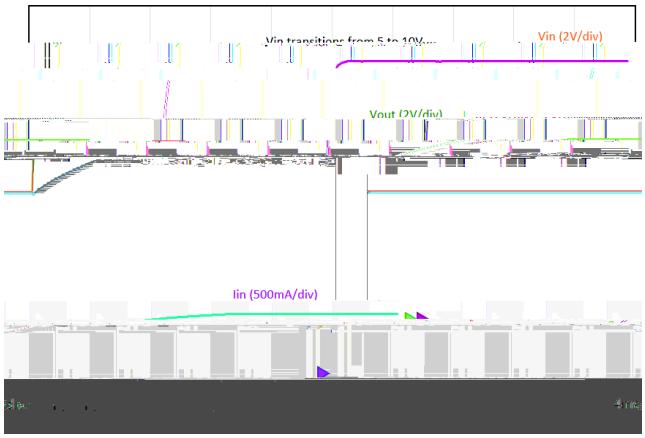
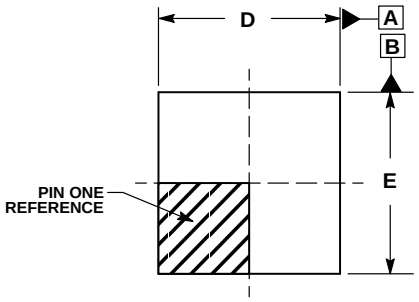


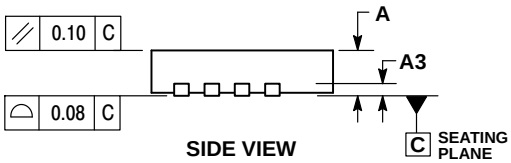
Figure 5. Output Voltage Protection

WDFNW10, 3x3, 0.5P

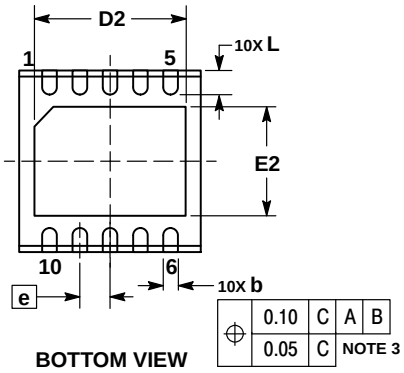
SCALE 2:1



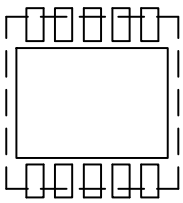
TOP VIEW



SIDE VIEW



BOTTOM VIEW



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