PYTHON 1.3/0.5/0.3 MegaPixels Global Shutter CMOS Image Sensors

NOIP1SN1300A

FEATURES

- , Size Options:
- PYTHON 300: 640 x 480 Active Pixels, 1/4" Optical Format
- PYTHON 500: 800 x 600 Active Pixels, 1/3.6" Optical Format
- PYTHON 1300: 1280 x 1024 Active Pixels, 1/2" Optical Format Data Output Options:
- Data Odiput Options.

 • P1_SN/SE/FN: 4 LVDS Data Channels.
 - PI-SN/SE/FIN. 4 LVDS Dat
 P2-SN/SE: 10 bit Parallel
 - P3-SN/SE/FN: 2 LVDS Data Channels
- 4.8 μm x 4.8

Readout Programmable Region of Interest (ROI)

- Serial Peripheral Interface (SPI)
- Automatic Exposure Control (AEC)
- Phase Locked Loop (PLL)
- High Dynamic Range (HDR) Modes Possible
- $\overline{}^{-}$ Dual Power Supply (3.3 V and 1.8 V)
- -40 C to +85 C Operational Temperature Range
- $\frac{1}{2}$ 48–pin LCC
- Power Dissipation:
 - ◆ 620 mW (P1, 4 LVDS, ZROT)
 - 420 mW (P1, P3, 2 LVDS, NROT)
 - 270 mW (P1, P3, 1 LVDS, NROT)
 - 420 mW (P2, ZROT)
- These Devices are Pb-Free and are RoHS Compliant



Figure 1. PYTHON 1300

APPLICATIONS

- Machine Vision
- __ Motion Monitoring
- Security
- Barcode Scanning (2D)

DESCRIPTION

The PYTHON 300, PYTHON 500, and PYTHON 1300 image sensors utilize high sensitivity $4.8 \,\mu m x \, 4.8 \,\mu m$ pixels that support low noise "pipelined" and "triggered" global shutter readout modes. The sensors support correlated double sampling (CDS) readout, reducing noise and increasing dynamic range.

The image sensors have on-chip programmable gain amplifiers and 10-bit A/D converters. The integration time and gain parameters can be reconfigured without any visible image artifact. Optionally the on-chip automatic exposure control loop (AEC) controls these parameters dynamically. The image's black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to eight regions can be programmed, achieving even higher frame rates.

The image data interface of the P1–SN/SE/FN devices consists of four LVDS lanes, enabling frame rates up to 210 frames per second in Zero ROT mode for the PYTHON 1300. Each channel runs at 720 Mbps. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receiving end. The P2–SN/SE devices provide a parallel CMOS output interface at reduced frame rate. The P3–SN/SE/FN devices are the same as the P1–SN/SE/FN but with only two of the four LVDS data channels enabled, facilitating frame rates of 90 frames per second in Normal ROT for the PYTHON 1300.

The devices are provided in a 48-pin LCC package and are available in monochrome, Bayer color, and extended near-infrared (NIR) configurations.

ORDERING INFORMATION

Part Number	Description	Package
PYTHON 1300		
NOIP1SN1300A QDI	1.3 Megapixel, Monochrome, LVDS Output	
NOIP1SE1300A QDI	1.3 Megapixel, Bayer Color, LVDS Output	
NOIP1FN1300A QDI	1.3 Megapixel, Monochrome with enhanced NIR, LVDS Output	
NOIP2SN1300A QDI	1.3 Megapixel, Monochrome, CMOS (parallel) Output	
NOIP2SE1300A QDI	1.3 Megapixel, Bayer Color, CMOS (parallel) Output	
NOIP1SN1300A QTI	1.3 Megapixel, Monochrome, LVDS Output, Protective Foil	
NOIP1SE1300A QTI	1.3 Megapixel, Bayer Color, LVDS Output, Protective Foil	40 aia 00
NOIP1FN1300A QTI	1.3 Megapixel, Monochrome with enhanced NIR, LVDS Output, Protective Foil	48 pin LCC
NOIP3SN1300A QDI	1.3 Megapixel, 2 LVDS Outputs, Monochrome	
NOIP3FN1300A QDI	1.3 Megapixel, 2 LVDS Outputs, NIR enhanced Monochrome	

SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

Parameter	Specification
Pixel type	In pixel CDS. Global shutter pixel architecture
Shutter type	Pipelined and triggered global shutter
Frame rate Zero ROT/ Normal ROT mode	P1 SN/SE/FN: PYTHON 300: 815/545 fps PYTHON 500: 545/385 fps PYTHON 1300: 210/165 fps P2 SN/SE: 50/43 fps P3 SN/SE/FN: NA/90 fps
Master clock	P1, P3 SN/SE/FN: 72 MHz when PLL is used, 360 MHz (10 bit) / 288 MHz (8 bit) when PLL is not used P2 SN/SE: 72 MHz
Windowing	8 Randomly programmable windows. Nor- mal, sub sampled and binned readout modes
ADC resolution	10 bit, 8 bit (Note 1)
LVDS outputs	P1 SN/SE/FN: 4/2/1 data + sync + clock P3 SN/SE/FN: 2/1 data + sync + clock
CMOS outputs	P2 SN/SE: 10 bit parallel output, frame_valid, line_valid, clock
Data rate	P1 SN/SE/FN: 4 x 720 Mbps (10 bit) / 4 x 576 Mbps (8 bit) P2 SN/SE: 72 Mhz P3 SN/SE/FN: 2 x 720 Mbps (10 bit)
Power dissipation (10 bit mode)	P1 SN/SE/FN: 620 mW (4 data channels) P1, P3 SN/SE/FN: 420 mW (2 data ch.) P1, P3 SN/SE/FN: 270 mW (1 data ch.) P2 SN/SE: 420 mW
Package type	48 pin LCC

Table 2. ELECTRO-OPTICAL SPECIFICATIONS

Parameter	Specification
Active pixels	PYTHON 300: 640 (H) x 480 (V) PYTHON 500: 800 (H) x 600 (V) PYTHON 1300: 1280 (H) x 1024 (V)
Pixel size	4.8 μm x 4.8 μm
Conversion gain	0.096 LSB10/e 140 μV/e
Dark temporal noise	< 9 e (Normal ROT, 1x gain) < 7 e (Normal ROT, 2x gain)
Responsivity at 550 nm	7.7 V/lux.s
Parasitic Light Sensitivity (PLS)	<1/8000
Full Well Charge	10000 e
Quantum Efficiency at 550 nm	56%
Pixel FPN	< 1.0 LSB10
PRNU	< 2% or 10 LSB10 on half scale response of 525LSB10
MTF	68% @ 535 nm X dir & Y dir
PSNL at 20 C	120 LSB10/s, 1200 e /s
Dark signal at 20 C	5 e /s, 0.5 LSB10/s
Dynamic Range	> 60 dB in global shutter mode
Signal to Noise Ratio (SNR max)	40 dB

Table 3. RECOMMENDED OPERATING RATINGS (Note 2)

Symbol	Description	Min	Max	Unit
TJ	Operating temperature range	40	85	С

6, 7, 8 and 9)

Min Typ	Max	Unit
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ternal 0 V ground reference.)

3.2	3.3	3.4	V
	140		mA
1.7	1.8	1.9	V
	80		mA
3.25	3.3	3.35	V
	5		mA

Unit

% ps



Color Filter Array

The PYTHON color sensors are processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left.



Figure 2. Color Filter Array for the Pixel Array



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Figure 4. Quantum Efficiency Curve for Standard and NIR Mono

Ray Angle and Microlens Array Information

An array of microlenses is placed over the CMOS pixel array in order to improve the absolute responsivity of the photodiodes. The combined microlens array and pixel array has two important properties:

1. Angular dependency of photoresponse of a pixel

The photoresponse of a pixel with microlens in the center of the array to a fixed optical power with varied incidence angle is as plotted in Figure 5, where definitions of angles ϕx and ϕy are as described by Figure 6.

2. Microlens shift across array and CRA

The microlens array is fabricated with a slightly smaller pitch than the array of photodiodes. This difference in pitch creates a varying degree of shift of a pixel's microlens with regards to its photodiode. A shift in microlens position versus photodiode position will cause a tilted angle of peak photoresponse, here denoted Chief Ray Angle (CRA). Microlenses and photodiodes are aligned with 0 shift and CRA in the center of the array, while the shift and CRA increases radially towards its edges, as illustrated by Figure 7.

The purpose of the shifted microlenses is to improve the uniformity of photoresponse when camera lenses with a finite exit pupil distance are used. The CRA varies nearly linearly with distance from the center as illustrated in Figure 8, with a corner CRA of approximately 2.7 degrees. This edge CRA is matching a lens with exit pupil distance of ~ 80 mm.



Figure 5. Central Pixel Photoresponse to a Fixed Optical Power with Incidence Angle varied along ϕ_x and ϕ_y



The center axes of the microlens and the photodiode coincide for the center pixels. For the edge pixels, there is a shift between the axes of the microlens and the photodiode causing a Peak Response Incidence Angle (CRA) that deviates from the normal of the pixel array.

Figure 7. Principles of Microlens Shift



Figure 8. Variation of Peak Responsivity Angle (CRA) as a Function of Distance from the Center of the Array



OVERVIEW

Figures 9



OPERATING MODES

Global Shutter Mode

The PYTHON 300, PYTHON 500, and PYTHON 1300 operate in pipelined or triggered global shuttering modes. In this mode, light integration, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 11 shows the integration and readout sequence



Integration Time Handling		Reset Exposure Time N		Reset N+1 Exposure T im e N+1]
Readout Handling	FOT	Readout N 1	FOT	Readout N	FOT
					Ŕ

Figure 13. Pipelined Shutter Operated in Slave Mode

Normal and Zero Row Overhead Time (ROT) Modes



SENSOR OPERATION

Flowchart

Figure 17 shows the sensor operation flowchart. The sensor has six different 'states'. Every state is indicated with the oval

Sensor States

Low Power Standby

In low power standby state, all power supplies are on, but internally every block is disabled. No internal clock is running (PLL / LVDS clock receiver is disabled).

All register settings are unchanged.

Only a subset of the SPI registers is active for read/write in order to be able to configure clock settings and leave the low power standby state. The only SPI registers that should be touched are the ones required for the 'Enable Clock Management' action described in Enable Clock Management – Part 1 on page 17

Standby (1)

In standby state, the PLL/LVDS clock receiver is running, but the derived logic clock signal is not enabled.

Standby (2)

In standby state, the derived logic clock signal is running. All SPI registers are active, meaning that all SPI registers can be accessed for read or write operations. All other blocks are disabled.

Idle

In the idle state, all internal blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images. The sensor can be operated in global master/slave modes.

User Actions: Power Up Functional Mode Sequences

Power Up Sequence

Figure 18 shows the power up sequence of the sensor. The figure indicates that the first supply to ramp-up is the vdd_18 supply, followed by vdd_33 and vdd_pix respectively. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. When the clock frequency is stable, the reset_n

Use of Phase Locked Loop

If PLL is used, the PLL is started after the upload of the SPI registers. The PLL requires (dependent on the settings) some time to generate a stable output clock. A lock detect circuit detects if the clock is stable. When complete, this is flagged in a status register.

NOTE: The lock detect status must not be checked for the P2



Sensor Reconfiguration

During the standby, idle, or running state several sensor parameters can be reconfigured.

- Frame Rate and Exposure Time: Frame rate and
- exposure time changes can occur during standby, idle, and running states by modifying registers 199 to 203. Refer to page 30-32 for more information.
- Signal Path Gain: Signal path gain changes can occur - during standby, idle, and running states by modifying registers 204/205. Refer to page 37 for more information.
- Windowing: Changes with respect to windowing can
- occur during standby, idle, and running states. Refer to Multiple Window Readout on page 26 for more information.
- Subsampling: Changes of the subsampling mode can
- occur during standby, idle, and running states by modifying register 192. Refer to Subsampling on page 27 for more information.
- _ Shutter Mode: The shutter mode can only be changed
- during standby or idle mode by modifying register 192. Reconfiguring the shutter mode during running state is not supported.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. Reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 15 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Group	Addresses	Description
Clock generator	32	Configure according to recommendation
Image core	40	Configure according to recommendation
AFE	48	Configure according to recommendation
Bias	64–71	Configure according to recommendation
LVDS	112	Configure according to recommendation
Sequencer mode selection	192 [6:1]	Operation modes are: _ triggered_mode _ slave_mode
All reserved registers		Keep reserved registers to their default state, unless otherwise described in the

Table 6. STATIC READOUT PARAMETERS

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shom9to some registers as



Table 9. ALTERNATE SYNC CONFIGURATIONS

Group	Affected Registers	Description
sync_black_lines	black_lines	Update of black line configuration is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.
sync_exposure	mult_timer fr_length exposure	Update of exposure configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.
sync_gain	mux_gainsw afe_gain	Update of gain configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.
sync_roi	roi_active0[7:0]	



Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ____ ss_n: Active Low Slave Select
- $\frac{1}{2}$ mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor's system clock. When the master wants to write or read a sensor's register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 22 shows the communication protocol for read and write accesses of the SPI registers. The PYTHON 300, PYTHON 500, and PYTHON 1300 image sensors use 9–bit addresses and 16–bit data words.

Data driven by the system is colored blue in Figure 16, while data driven by the sensor is colored yellow. The data in grey indicates high–Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

- 3. Select the sensor for read or write by pulling down the ss_n line.
- 4. One SPI clock cycle after selecting the sensor, the 9-bit data is transferred, most significant bit first.

The sck clock is passed through to the sensor as indicated in Figure 22. The sensor samples this data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock).

- 5. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
- 6. Data transmission:
- For write commands, the master continues sending the 16-bit data, most significant bit first.
- For read commands, the sensor returns the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
- 7. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Note that the maximum frequency for the SPI interface scales with the input clock frequency, bit depth and LVDS output multiplexing as described in Table 5.

Consecutive SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.



Figure 22. SPI Read and Write Timing Diagram

Table 11. SPI TIMING REQUIREMENTS

Group	Addresses	Description	Units
tsck	sck clock period	100 (*)	ns
tsssck	ss_n low to sck rising edge	tsck	ns
tsckss	sck falling edge to ss_n high	tsck	ns
ts_mosi	Required setup time for mosi	20	ns
th_mosi	Required hold time for mosi	20	ns
ts_miso	Setup time for miso	tsck/2 10	ns
th_miso	Hold time for miso	tsck/2 20	ns
tspi	Minimal time between two consecutive SPI accesses (not shown in figure)	2 x tsck	ns

*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as 1/f_{SPI}. See text for more information on SPI clock frequency restrictions.

IMAGE SENSOR TIMING AND READOUT

The following sections describe the configurations for single slope reset mechanism. Dual and triple slope handling during global shutter operation is similar to the single slope operation. Extra integration time registers are available.

Global Shutter Mode

Pipelined Global Shutter (Master)

The integration time is controlled by the registers fr_length[15:0] and exposure[15:0]. The mult_timer configuration defines the granularity of the registers reset_length and exposure. It is read as number of system clock cycles (14.706 ns nominal at 68 MHz) for the P1–SN/SE/FN, P3–SN/SE/FN version and 18 MHz cycles (55.556 ns nominal) for the P2–SN/SE version.

The exposure control for (Pipelined) Global Master mode is depicted in Figure 23.

The pixel values are transferred to the storage node during FOT, after which all photo diodes are reset. The reset state remains active for a certain time, defined by the reset_length and mult_timer registers, as shown in the figure. Note that meanwhile the image array is read out line by line. After this

reset period, the global photodiode reset condition is abandoned. This indicates the start of the integration or exposure time. The length of the exposure time is defined by the registers exposure and mult_timer.

NOTE: The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.

Make sure that the sum of the reset time and exposure

- time exceeds the time required to readout all lines. If this is not the case, the exposure time is extended until all (active) lines are read out.
- Alternatively, it is possible to specify the frame time and exposure time. The sensor automatically calculates
- the required reset time. This mode is enabled by the fr_mode register. The frame time is specified in the register fr_length.







Binning

Pixel binning is a technique in which different pixels belonging to a rectangular bin are averaged in the analog domain. Two-by-two pixel binning is available with the monochrome



Automatic Exposure Control

The exposure control mechanism has the shape of a general feedback control system. Figure 30 shows the high level block diagram of the exposure control loop.



Figure 30. Automatic Exposure Control Loop

Target Illumination The target illumination value is configured by means of register *desired_intensity* as shown in Table 14.

Table 14. AEC TARGET ILLUMINATION CONFIGURATION

Register

AEC Control Range

The control range for each of the exposure parameters can be pre-programmed in the sensor. Table 16 lists the relevant registers.

Table 16. MINIMUM AND MAXIMUM EXPOSURE CONTROL PARAMETERS

Register	Name	Description
168[15:0]	min_exposure	Lower bound for the integration time applied by the AEC
169[1:0]	min_mux_gain	Lower bound for the first stage analog amplifier. This stage has three configurations with the following approximative gains: 0x0 = 1x 0x1 = 2x 0x2 = 4x
169[3:2]	min_afe_gain	Lower bound for the second stage analog amplifier. This stage has one configuration with the following approximative gain: 0x0 = 1.00x
169[15:4]	min_digital_gain	Lower bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format
170[15:0]	max_exposure	Upper bound for the integration time applied by the AEC
171[1:0]	max_mux_gain	Upper bound for the first stage analog amplifier. This stage has three configurations with the following approximative gains: 0x0 = 1x 0x1 = 2x 0x2 = 4x
171[3:2]	max_afe_gain	Upper bound for the second stage analog amplifier This stage has one configuration with the following approximative gain: 0x0 = 1.00x
171[15:4]	max_digit- al_gain	Upper bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format

AEC Update Frequency

As an integration time update has a latency of one frame, the exposure control parameters are evaluated and updated every other frame.

Note: The gain update latency must be postpone to match the integration time latency. This is done by asserting the *gain_lat_comp* register on address 204[13].

Exposure Control Status Registers

Configured7 -1.1962 TD710 1 Tf9 0 onfi-f9 0 0 9 317-.evuated and up

Register	Name	Description	
Sequencer Status Registers			
242[15:0]	mult_timer	mult_timer for current frame (global shutter only). Note: this parameter is updated once it takes effect on the image.	
243[15:0]	reset_length	Image array reset length for the current frame (global shutter only). Note: this parameter is updated once it takes effect on the image.	
244[15:0]	exposure	Exposure for the current frame. Note: this parameter is updated once it takes effect on the image.	
245[15:0]	exposure_ds	Dual slope exposure for the current frame. Note this parameter is not controlled by the AEC. Note: this parameter is updated once it takes effect on the image.	
246[15:0]	exposure_ts	Triple slope exposure for the current frame. Note this parameter is not controlled by the AEC. Note: this parameter is updated once it takes effect on the image.	
247[4:0]	mux_gainsw	1 st stage analog gain for the current frame. Note: this parameter is updated once it takes effect on the image.	

Table 17. EXPOSURE CONTROL STATUS REGISTERS

Register	Name	Description
247[12:5]	afe_gain	2 nd stage analog gain for the cur- rent frame. Note: this parameter is updated once it takes effect on the image.
248[11:0]	db_gain	Digital gain configuration for the current frame (5.7 unsigned format). Note: this parameter is updated once it takes effect on the image.
248[12]	dual_slope	Dual slope configuration for the current frame Note 1 : this parameter is updated once it takes effect on the image. Note 2 : This parameter is not controlled by the AEC.
248[13]	triple_slope	Triple slope configuration for the current frame. Note 1 : this parameter is updated once it takes effect on the image. Note 2 : This parameter is not controlled by the AEC.



Mode Changes and Frame Blanking

Dynamically reconfiguring the sensor may lead to corrupted or non-uniformilly exposed frames. For some reconfigurations, the sensor automatically blanks out the image data during one frame. Frame blanking is summarized in the following table for the sensor's image related modes.



DATA OUTPUT FORMAT

The PYTHON 300, PYTHON 500, and PYTHON 1300 image sensors are available in two LVDS output configuration, P1 and P3.

The P1 configuration utilizes four LVDS output channels together with an LVDS clock output and an LVDS synchronization output channel.

The P3 configuration consists of two LVDS output channels together with an LVDS clock output and an LVDS synchronization output channel.

The PYTHON 1300 is also available in a CMOS output configuration – P2, which includes a 10–bit parallel CMOS output together with a CMOS clock output and 'frame valid' and 'line valid' CMOS output signals.

P1-SN/SE/FN, P3-SN/SE/FN: LVDS Interface Version

LVDS Output Channels

The image data output occurs through four LVDS data channels where a synchronization LVDS channel and an LVDS output clock signal synchronizes the data. Referring to Table 21, the four data channels on the P1 option are used to output the image data only, while on the P3 option, two data channel channels are utilized. The sync channel transmits information about the data sent over these data channels (includes codes indicating black pixels, normal pixels, and CRC codes).

8-bit / 10-bit Mode

The sensor can be used in 8-bit or 10-bit mode. In 10-bit mode, the words on data and sync channel have

a 10-bit length. The output data rate is 720 Mbps. In 8-bit mode, the words on data and sync channel have

an 8-bit length, the output data rate is 576 Mbps.

Note that the 8-bit mode can only be used to limit the data rate at the consequence of image data word depth. It is not supported to operate the sensor in 8-bit mode at a higher clock frequency to achieve higher frame rates.

The P1 option supports 10-bit/8-bit in ZROT/NROT mode, while the P3 option supports 10-bit NROT mode only.

Frame Format

The frame format in 8-bit mode is identical to the 10-bit mode with the exception that the Sync and data word depth is reduced to eight bits.

The frame format in 10-bit mode is explained by example of the readout of two (overlapping) windows as shown in Figure 31(a).

The readout of a frame occurs on a line-by-line basis. The read pointer goes from left to right, bottom to top.

Figure 31 indicates that, after the FOT is completed, the sensor reads out a number of black lines for black calibration purposes. After these black lines, the windows are processed. First a number of lines which only includes information of 'ROI 0' are sent out, starting at position y0_start. When the line at position y1_start is reached, a number of lines containing data of 'ROI 0' and 'ROI 1' are sent out, until the line position of y0_end is reached. From there on, only data of 'ROI 1' appears on the data output channels until line position y1_end is reached

During read out of the image data over the data channels, the sync channel sends out frame synchronization codes which give information related to the image data that is sent over the four data output channels.

Each line of a window starts with a Line Start (LS) indication and ends with a Line End (LE) indication. The line start of the first line is replaced by a Frame Start (FS);

Figure 31. P1-
Figure 33 shows shows the details of the readout of a number of lines for single window readout, at the beginning of the frame.



Figure 33. P1–SN/SE/FN, P3–SN/SE/FN: Time Line for Single Window Readout (at the start of a frame)



Window Identification
Frame synchronization codes are always followed by a 3-bit window identification (bits 2:0). This is an integer number, ranging from 0 to 7, indicating the active window.





Data Order for P1–SN/SE/FN, P3–SN/SE/FN: LVDS Interface Version

To read out the image data through the output channels, the pixel array is organized in kernels. The kernel size is eight pixels in x-direction by one pixel in y-direction. The data order in 8-bit mode is identical to the 10-bit mode. Figure 35 indicates how the kernels are organized. The first kernel (kernel [0, 0]) is located in the bottom left corner. The data order of this image data on the data output channels depends on the subsampling mode.



Figure 35. Kernel Organization in Pixel Array

- P1-SN/SE/FN, P3-SN/SE/FN: Subsampling disabled
- 4 LVDS output channels (P1 only)

The image data is read out in kernels of eight pixels in x-direction by one pixel in y-direction. One data channel output delivers two pixel values of one kernel sequentially.

Figure 36 shows how a kernel is read out over the four output channels. For even positioned kernels, the kernels are read out ascending, while for odd positioned kernels the data order is reversed (descending).



Figure 36. P1-SN/SE/FN: 4 LVDS Data Output Order when Subsampling is Disabled

• 2 LVDS output channels

Figure 37 shows how a kernel is read out over 2 output channels. Each pair of adjacent channels is multiplexed into one channel. For even positioned kernels, the kernels are

read out ascending but in pair of even and odd pixels, while for odd positioned kernels the data order is reversed (descending) but in pair of even and odd pixels.

kernel N 2 kernel N	kernel N	kernel N+1
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Figure 37. P1–SN/SE/FN, P3–SN/SE/FN: 2 LVDS Data Output Order when Subsampling is Disabled

P1-SN/FN, P3-SN/FN: Subsampling on Monochrome Sensor

During subsampling on a monochrome sensor, every other pixel is read out and the lines are read in a read-1-skip-1 manner. To read out the image data with subsampling enabled on a monochrome sensor, two neighboring kernels are combined to a single kernel of 16 pixels in the x-direction and one pixel in the y-direction. Only the pixels at the even pixel positions inside that kernel are read out. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout.

• 4 LVDS output channels (P1 only)

Figure 39 shows the data order for 4 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout



• 2 LVDS output channels

Figure 43 shows the data order for 2 LVDS output channels. Note that there is no difference in data order for

pixel #

0 13 1 12 4

even/odd kernel numbers, as opposed to the 'no-subsampling' readout described in previous section.

kernel N 2	kernel N 1	kernel N	kernel N+1		
		*			

Figure 43. P1–SE, P3–SE: Data Output Order for 2 LVDS Output Channels in Subsampling Mode on a Color Sensor



P2-SN/SE: CMOS Interface Version

CMOS Output Signals

The image data output occurs through a single 10-bit parallel CMOS data output, operating at the applied dk_pll frequency. A CMOS clock output, 'frame valid' and 'line valid' signal synchronizes the output data.

No windowing information is sent out by the sensor.

8-bit/10-bit Mode

The 8-bit mode is not supported when using the parallel CMOS output interface.

Frame Format

Frame timing is indicated by means of two signals: frame_valid and line_valid.

- The frame_valid indication is asserted at the start of a
- new frame and remains asserted until the last line of the frame is completely transmitted.
- The line_valid indication serves the following needs:
 - While the line_valid indication is asserted, the data channels contain valid pixel data.
 - The line valid communicates frame timing as it is asserted at the start of each line and it is de-asserted at the end of the line. Low periods indicate the idle time between lines (ROT).
 - The data channels transmit the calculated CRC code after each line. This can be detected as the data words right after the falling edge of the line valid.



Figure 45. P2–SN/SE/FN: Frame Timing Indication

The frame format is explained with an example of the readout of two (overlapping) windows as shown in Figure 46 (a).

The readout of a frame occurs on a line-by-line basis. The read pointer goes from left to right, bottom to top. Figure 46 (a) and (b) indicate that, after the FOT is finished, a number of lines which include information of 'ROI 0' are sent out,

starting at position y0_start. When the line at position y1_start is reached, a number of lines containing data of 'ROI 0' and 'ROI 1' are sent out, until the line position of y0_end is reached. Then, only data of 'ROI 1' appears on the data output until line position y1_end is reached. The line_valid strobe is not shown in Figure 46.



(a)





Data order for P2-SN/SE: CMOS Interface Version

To read out the image data through the parallel CMOS output, the pixel array is divided in kernels. The kernel size is eight pixels in x-direction by one pixel in y-direction. Figure 35 on page 40 indicates how the kernels are organized.

The data order of this image data on the data output channels depends on the subsampling mode.

- P2-SN/SE: No Subsampling
- The image data is read out in kernels of eight pixels in x-direction by one pixel in y-direction.

Figure 47 shows the pixel sequence of a kernel which is read out over the single CMOS output channel. The pixel order is different for even and odd kernel positions.



Figure 47. P2-SN/SE: Data Output Order without Subsampling

P2-SN: Subsampling On Monochrome Sensor

To read out the image data with subsampling enabled on a monochrome sensor, two neighboring kernels are combined to a single kernel of 16 pixels in the x-direction and one pixel in the y-direction. Only the pixels at the even pixel positions inside that kernel are read out. Figure 48 shows the data order

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout.



Figure 48. P2–SN: Data Output Order with Subsampling on a Monochrome Sensor

P2-SE: Subsampling On Color Sensor

 To read out the image data with subsampling enabled on a color sensor, two neighboring kernels are combined to a single kernel of 16 pixels in the x-direction and one pixel in

the y-direction. Only the pixels 0, 1, 4, 5, 8, 9, 12, and 13 are read out. Figure 49 shows the data order.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout.



Figure 49. P2–SE: Data Output Order with Subsampling on a Color Sensor





Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Туре
1	17		reserved	0x2113	8467	Reserved	RW
		[7:0]	reserved	0x13	19	Reserved	
		[12:8]	reserved	0x1	1	Reserved	
		[14:13]	reserved	0x1	1	Reserved	

I/O [Block Offset: 20]

config1	0x0000	0	IO Configuration	RW
clock_in_pwd_n	0x0	0	Power down Clock Input	
reserved	0x0	0	Reserved	



Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Туре
		[2]	colbias_enable	0x0	0	Bias Enable '0': disabled '1': enabled	
1	41		image_core_config1	0x0B5A	2906	Image Core Configuration	RW
		[3:0]	dac_ds	0xA	10	Double Slope Reset Level	
		[7:4]	dac_ts	0x5	5	Triple Slope Reset Level	
		[10:8]	reserved	0x3	3	Reserved	
		[12:11]	reserved	0x1	1	Reserved	
		[13]	reserved	0x0	0	Reserved	
		[14]					

Table 28. REGISTER MAP

Address Offset



Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Туре
6	118		sync_code1	0x0015	21	Data Formating - BL Indication	RW
		[9:0]	bl_0	0x015	21	Black Pixel Identification Sync Code - Even kernels	
7	119		sync_code2	0x0035	53	Data Formating - IMG Indication	RW
		[9:0]	img_0	0x035	53	Valid Pixel Identification Sync Code - Even kernels	
8	120		sync_code3	0x0025	37	Data Formating - IMG Indication	RW
		[9:0]	ref_0	0x025	37	Reference Pixel Identification Sync Code -	

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default		Туре
2	130			0x000F	15		RW
				0x1	1	Assert ivalid for black lines when '1', gate frame_valid for black lines when '0'. Parallel output mode only.	
				0x1	1	Assert line_valid for black lines when '1', gate line_valid for black lines when '0'. Parallel output mode only.	
				0x1	1	Assert frame_valid for ref lines when '1', gate frame_valid for black lines when '0'. Parallel output mode only.	
				0x1	1	Assert line_valid for ref lines when '1', gate line_valid for black lines when '0'. Parallel output mode only.	
				0x0	0	Behaviour om3 29.707 ref357.449 594273.77 560	68033 5

IAP						
t Field	Register Name	Default (Hex)	Default	Description	Туре	
	test_configuration1	0x0302	770	Data Formating Test Configuration	RW	
[7:0]	testpattern2_lsb	0x02	2	Testpattern used on datapath #2 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.		
15:8]	testpattern3_lsb	0x03	3	Testpattern used on datapath #3 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.		
	reserved	0x0504	1284	Reserved	RW	
[7:0]	reserved	0x04	4	Reserved		
15:8]	reserved	0x05	5	Reserved		
	reserved	0x0706	1798	Reserved	RW	
[7:0]	reserved	0x06	6	Reserved		
15:8]	reserved	0x07	7	Reserved		
	test_configuration16	0x0000	0	Data Formating Test Configuration	RW	
[1:0]	testpattern0_msb	0x0	0	Testpattern used when testpattern_en = '1'		
[3:2]	testpattern1_msb	0x0	0	Testpattern used when testpattern_en = '1'		
[5:4]	testpattern2_msb	0x0	0	Testpattern used when testpattern_en = '1'		
[7:6]	testpattern3_msb	0x0	0	Testpattern used when testpattern_en = '1'		
[9:8]	reserved	0x0	0	Reserved		
1:10]	reserved	0x0	0	Reserved		
3:12]	reserved	0x0	0	Reserved		
5:14]	reserved	0x0	0	Reserved		
	reserved	0x0000	0	Reserved	RW	
15:0]	reserved	0x0000	0	Reserved		
	reserved	0x0000	0	Reserved	RW	
15:0]	reserved	0x0000	0	Reserved		
	configuration	0x0010	16	AEC Configuration	RW	
[0]	enable	9x0	0	AEC Enable		
[1]	restart_filter	0x0	0	Restart AEC filter		
[2]	freeze	0x0	0	Freeze AEC filter and enforcer gains		
[3]	pixel_valid	0x0	0	Use every pixel from channel when 0, every 4th pixel when 1		
[4]	amp_pri	0x1	1	Column amplifier gets higher priority than AFE PGA in gain distribution if 1. Vice versa if 0		

www.onser

0x60B8

intensity

55



Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Туре
20	180		reserved	0x0100	256	Reserved	RW

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Туре
		[15]	reserved	0x0	0	Reserved	
1	193						





Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Туре
		[12:8]	gate_first_line	0x1	1	Blank out first lines 0: no blank 1-31: blank 1-31 lines	
6	198		reserved	0x0000	0	Reserved	RW
		[11:0]	reserved	0x000	0	Reserved	
7	199		mult_timer0	0x0001	1	Exposure/Frame Rate Configuration	RW
		1			-		



(Hex)

Table 28. REGISTER MAP

Address Offset

Default

Default

Description

Туре

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Туре
4	260		roi1_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
5	261		roi1_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
6	262		roi2_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
7	263		roi2_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
8	264		roi2_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
9	265		roi3_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
10	266		roi3_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
11	267		roi3_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
12	268		roi4_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
13	269		roi4_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
14	270		roi4_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
15	271		roi5_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
16	272		roi5_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
17	273		roi5_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
18	274		roi6_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
19	275		roi6_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
20	276		roi6_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
21	277		roi7_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	1
22	278		roi7_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	



Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Туре
23	279		roi7_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	

Sequencer ROI [Block Offset: 384]

0	384		reserved		Reserved	RW
		[15:0]	reserved		Reserved	
					:	
127	511		reserved		Reserved	RW
		[15:0]	reserved		Reserved	



PACKAGE INFORMATION

Pin List

The PYTHON 300, PYTHON 500, and PYTHON 1300 image sensors are available in an LVDS output configuration (P1-SN/SE/FN, P3-SN/SE/FN), with the PYTHON 1300 also available in a CMOS output configuration (P2-SN/SE). The LVDSI/Os comply to the TIA/EIA-644-A Standard and the CMOSI/Os have a 3.3 V signal level. Tables 29 and 30 show the pin list for both versions.

Table 29.	PIN LIST FOR	P1-SN/SE/FN.	P3-SN/SE/FN L	VDS INTERFACE
14010 20.				

Pack Pin No.	Pin Name	I/O Type	Direction	Description	
1	vdd_33	Supply		3.3 V Supply	
2	mosi	CMOS	Input	SPI Master Out Slave In	
3	miso	CMOS	Output	SPI Master In Slave Out	
4	sck	CMOS	Input	SPI Clock	
5	gnd_18	Supply		1.8 V Ground	
6	vdd_18	Supply		1.8 V Supply	
7	clock_outn	LVDS	Output	LVDS Clock Output (Negative)	
8	clock_outp	LVDS	Output	LVDS Clock Output (Positive)	
9	doutn0	LVDS	Output	LVDS Data Output Channel #0 (Negative)	
10	doutp0	LVDS	Output	LVDS Data Output Channel #0 (Positive)	
11	doutn1	LVDS	Output	LVDS Data Output Channel #1 (Negative). Not connected for P3	
12	doutp1	LVDS	Output	LVPS Data Output Channel #1 (Positive). Not connected for P3	
13	doutn2	LVDS	Output	LVDS Data Output Channel #2 (Negative)	
14					

Table 29. PIN LIST FOR P1-SN/SE/FN, P3-SN/SE/FN LVDS INTERFACE

Pack Pin No.	Pin Name	I/О Туре	Direction	Description
36	•			

Table 30. PIN LIST FOR P2–SN/SE CMOS INTERFACE

Pack Pin No.	Pin Name	I/O Type	Direction	Description
26	vdd_18	Supply		1.8 V Supply
27	gnd_18	Supply		1.8 V Ground
28	ibias_master	Analog	I/O	-

Parameter Min Max Units Description Тур Die Die thickness 725 μm (Refer to Figure 51 $\rm mm^2$ Die Size 9.0 X 7.95 and Figure 52 showing Pin 1 reference as left Die center, X offset to the center of package 50 0 50 μm Die center, Y offset to the center of the package 225 175 125 center) μm Die position, tilt to the Die Attach Plane 1 0 1 deg Die rotation accuracy (referenced to die scribe and lead fin-gers on package on all four sides) 1 0 1 deg Optical center referenced from the die/package center (X dir) 179.24 μm Optical center referenced from the die center (Y dir) 1542.14 μm Optical center referenced from the package center (Y dir) 1367.14 μm Distance from bottom of the package to top of the die surface 1.165 1.260 1.405 mm 0.655 Distance from top of the die surface to top of the glass lid 0.990 1.305 mm Glass Lid mm² XY size 13.6 X 13.6 Specification Thickness 0.5 0.55 0.6 mm Spectral response range 400 1000 nm

Table 31. MECHANICAL SPECIFICATION





Figure 50. Package Drawing for the 48-pin LCC Package



Table 32. OPTICAL CENTER INFORMATION

		PYTHON1300		PYTH	ION500	PYTHON300	
	References*	X (μm)	Υ (μm)	X (μm)	Υ (μm)	X (μm)	Υ (μm)
Die Outer	D1	0	9000	0	9000	0	9000
Cordinates	D2	7950	9000	7950	9000	7950	9000
	D3	7950	0	7950	0	7950	0
	D4	0	0	0	0	0	0
Die Center	CD	3975	4500	3975	4500	3975	4500
Pixel Area Coordinates	A1	704.56	8518.94	704.56	8518.94	704.569000	0




Packing and Tray Specification

The PYTHON packing specification with onsemi packing labels is packed as follows:

Table 33. PACKING AND TRAY SPECIFICATION

CLCC	Package (mm)			Tray	Restraint	Box
Leads	Length	Width	Thickness*			





Figure 54. Packing and Tray Configuration (2 of 2)



Glass Lid

The PYTHON 300, PYTHON 500, and PYTHON 1300 image sensors use a glass lid without any coatings. Figure 44 shows the transmission characteristics of the glass lid.

As shown in Figure 49, no infrared attenuating color filter glass is used. Use of an IR cut filter is recommended in the optical path when color devices are used. (source: http://www.pgo-online.com).



Figure 55. Transmission Characteristics of the Glass Lid

Protective Foil

For certain size and speed options, the sensor can be delivered with a protective foil that is intended to be

removed after assembly. The dimensions of the foil are as illustrated in Figure 56 with the tab aligned towards pin 1 of the package.



(units in mm) Figure 56. Dimensions of the Protective Foil



SPECIFICATIONS AND USEFUL REFERENCES

The following references are available to customers under NDA at the onsemi Image Sensor Portal:

For quality and reliability information, please download the Quality & Reliability

Product Acceptance Criteria

- с -Product Qualification Report
- L PYTHON Developer's Guide AND9362/D

Material Composition is available at

http://www.onsemi.com/PowerSolutions/MaterialCompos ition.do?searchParts=PYTHON1300

Useful References

For information on ESD handling, cover glass care and cleanliness, mounting information, please download the Image Sensor Handling and Best Practices Application Note (AN52561/D) from www.onsemi.com.



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