PYTHON 1.3/0.5/0.3 MegaPixels Global Shutter CMOS Image Sensors

NOIP1SN1300A

Figure 1. PYTHON 1300

FEATURES

APPLICATIONS

DESCRIPTION

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ORDERING INFORMATION

Part Number	Description	Package
PYTHON 1300		
NOIP1SN1300A QDI	1.3 Megapixel, Monochrome, LVDS Output	48 pin LCC
NOIP1SE1300A QDI	1.3 Megapixel, Bayer Color, LVDS Output	
NOIP1FN1300A QDI	1.3 Megapixel, Monochrome with enhanced NIR, LVDS Output	
NOIP2SN1300A QDI	1.3 Megapixel, Monochrome, CMOS (parallel) Output	
NOIP2SE1300A QDI	1.3 Megapixel, Bayer Color, CMOS (parallel) Output	
NOIP1SN1300A QTI	1.3 Megapixel, Monochrome, LVDS Output, Protective Foil	
NOIP1SE1300A QTI	1.3 Megapixel, Bayer Color, LVDS Output, Protective Foil	
NOIP1FN1300A QTI	1.3 Megapixel, Monochrome with enhanced NIR, LVDS Output, Protective Foil	
NOIP3SN1300A QDI	1.3 Megapixel, 2 LVDS Outputs, Monochrome	
NOIP3FN1300A QDI	1.3 Megapixel, 2 LVDS Outputs, NIR enhanced Monochrome	

SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

Parameter	Specification
Pixel type	In pixel CDS. Global shutter pixel architecture
Shutter type	Pipelined and triggered global shutter
Frame rate Zero ROT/ Normal ROT mode	P1 SN/SE/FN: PYTHON 300: 815/545 fps PYTHON 500: 545/385 fps PYTHON 1300: 210/165 fps P2 SN/SE: 50/43 fps P3 SN/SE/FN: NA/90 fps
Master clock	P1, P3 SN/SE/FN: 72 MHz when PLL is used, 360 MHz (10 bit) / 288 MHz (8 bit) when PLL is not used P2 SN/SE: 72 MHz
Windowing	8 Randomly programmable windows. Normal, sub sampled and binned readout modes
ADC resolution	10 bit, 8 bit (Note 1)
LVDS outputs	P1 SN/SE/FN: 4/2/1 data + sync + clock P3 SN/SE/FN: 2/1 data + sync + clock
CMOS outputs	P2 SN/SE: 10 bit parallel output, frame_valid, line_valid, clock
Data rate	P1 SN/SE/FN: 4 x 720 Mbps (10 bit) / 4 x 576 Mbps (8 bit) P2 SN/SE: 72 Mhz P3 SN/SE/FN: 2 x 720 Mbps (10 bit)
Power dissipation (10 bit mode)	P1 SN/SE/FN: 620 mW (4 data channels) P1, P3 SN/SE/FN: 420 mW (2 data ch.) P1, P3 SN/SE/FN: 270 mW (1 data ch.) P2 SN/SE: 420 mW
Package type	48 pin LCC

Table 2. ELECTRO−OPTICAL SPECIFICATIONS

Parameter	Specification
Active pixels	PYTHON 300: 640 (H) x 480 (V) PYTHON 500: 800 (H) x 600 (V) PYTHON 1300: 1280 (H) x 1024 (V)
Pixel size	4.8 μm x 4.8 μm
Conversion gain	0.096 LSB10/e 140 μV/e
Dark temporal noise	< 9 e (Normal ROT, 1x gain) < 7 e (Normal ROT, 2x gain)
Responsivity at 550 nm	7.7 V/lux.s
Parasitic Light Sensitivity (PLS)	<1/8000
Full Well Charge	10000 e
Quantum Efficiency at 550 nm	56%
Pixel FPN	< 1.0 LSB10
PRNU	< 2% or 10 LSB10 on half scale response of 525LSB10
MTF	68% @ 535 nm X dir & Y dir
PSNL at 20 C	120 LSB10/s, 1200 e /s
Dark signal at 20 C	5 e /s, 0.5 LSB10/s
Dynamic Range	> 60 dB in global shutter mode
Signal to Noise Ratio (SNR max)	40 dB

Table 3. RECOMMENDED OPERATING RATINGS (Note 2)

Symbol	Description	Min	Max	Unit
T_J	Operating temperature range	40	85	C

6, 7, 8 and 9)

Min	Typ	Max	Unit

ternal 0 V ground reference.)

3.2	3.3	**3.4**	V
	140		mA
1.7	1.8	**1.9**	V
	80		mA
3.25	3.3	**3.35**	V
	5		mA

Unit
MHz
%
ps

Color Filter Array

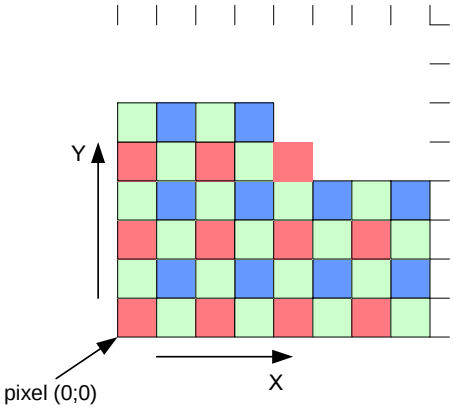

Figure 2. Color Filter Array for the Pixel Array

Figure 4. Quantum Efficiency Curve for Standard and NIR Mono

Ray Angle and Microlens Array Information

ϕ

ϕ

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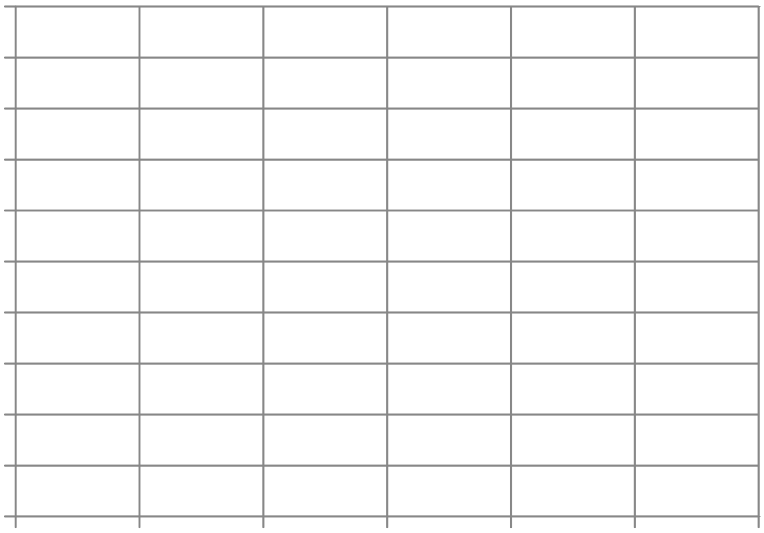
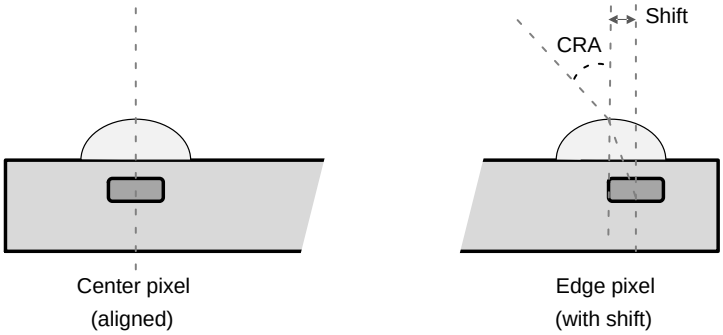


Figure 5. Central Pixel Photoresponse to a Fixed Optical Power with Incidence Angle varied along ϕ_x and ϕ_y



The center axes of the microlens and the photodiode coincide for the center pixels. For the edge pixels, there is a shift between the axes of the microlens and the photodiode causing a Peak Response Incidence Angle (CRA) that deviates from the normal of the pixel array.

Figure 7. Principles of Microlens Shift

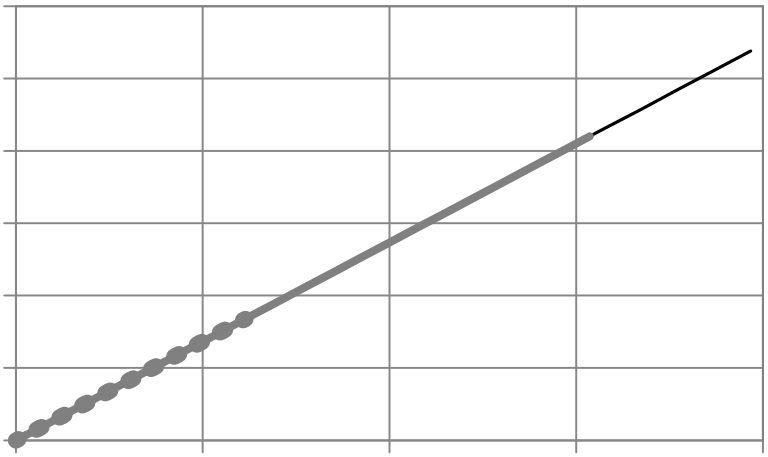


Figure 8. Variation of Peak Responsivity Angle (CRA) as a Function of Distance from the Center of the Array

OVERVIEW

OPERATING MODES

Global Shutter Mode

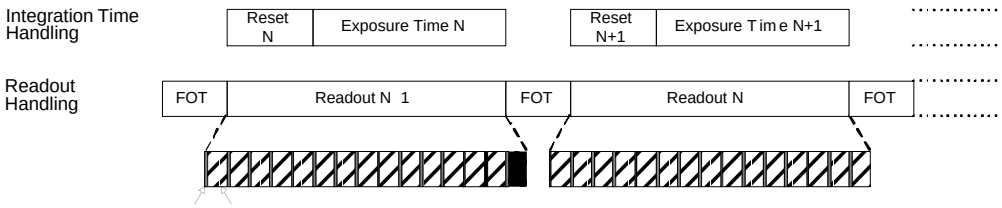


Figure 13. Pipelined Shutter Operated in Slave Mode

Normal and Zero Row Overhead Time (ROT) Modes

SENSOR OPERATION

Flowchart

Sensor States

Low Power Standby

Standby (1)

Standby (2)

Idle

Running

User Actions: Power Up Functional Mode Sequences

Power Up Sequence

Use of Phase Locked Loop

Sensor Reconfiguration

Sensor Configuration

Static Readout Parameters

Table 6. STATIC READOUT PARAMETERS

Group	Addresses	Description
Clock generator	32	Configure according to recommendation
Image core	40	Configure according to recommendation
AFE	48	Configure according to recommendation
Bias	64–71	Configure according to recommendation
LVDS	112	Configure according to recommendation
Sequencer mode selection	192 [6:1]	Operation modes are: triggered_mode slave_mode
All reserved registers		Keep reserved registers to their default state, unless otherwise described in the

Dynamic Readout Parameters

Table 9. ALTERNATE SYNC CONFIGURATIONS

Group	Affected Registers	Description
sync_black_lines	black_lines	Update of black line configuration is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_exposure	mult_timer fr_length exposure	Update of exposure configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_gain	mux_gainsw afe_gain	Update of gain configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_roi	roi_active0[7:0]	

Serial Peripheral Interface

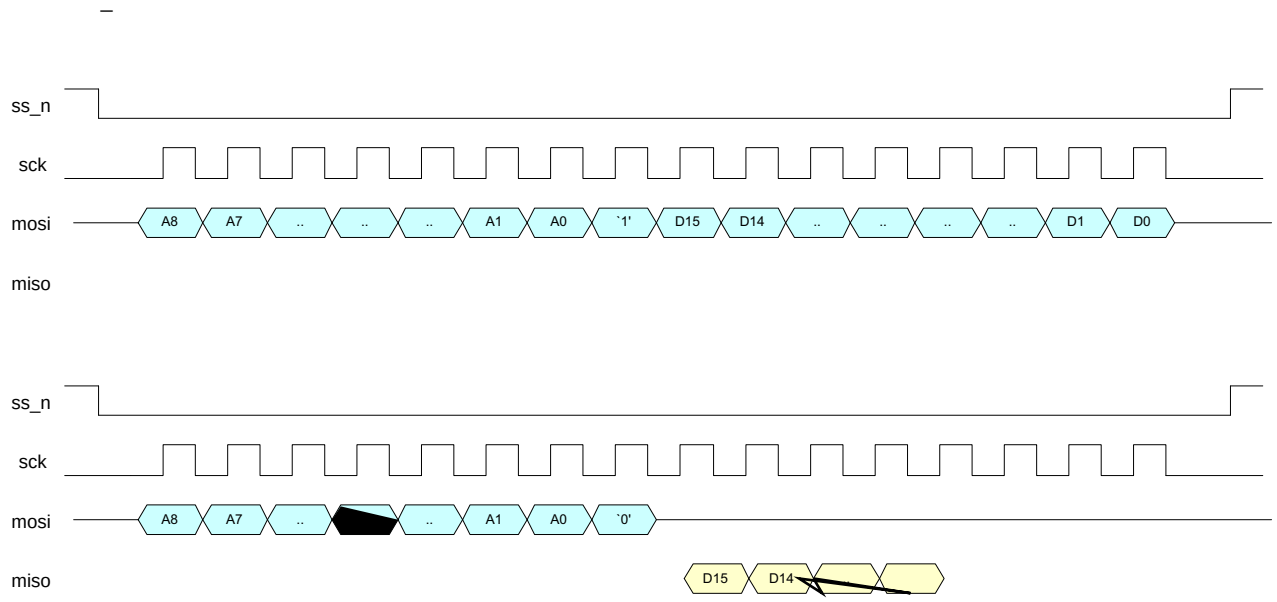


Figure 22. SPI Read and Write Timing Diagram

Table 11. SPI TIMING REQUIREMENTS

Group	Addresses	Description	Units
tsck	sck clock period	100 (*)	ns
tsssck	ss_n low to sck rising edge	tsck	ns
tsckss	sck falling edge to ss_n high	tsck	ns
ts_mosi	Required setup time for mosi	20	ns
th_mosi	Required hold time for mosi	20	ns
ts_miso	Setup time for miso	tsck/2 10	ns
th_miso	Hold time for miso	tsck/2 20	ns
tspi	Minimal time between two consecutive SPI accesses (not shown in figure)	2 x tsck	ns

*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as $1/f_{SPI}$. See text for more information on SPI clock frequency restrictions.

IMAGE SENSOR TIMING AND READOUT

Global Shutter Mode

Pipelined Global Shutter (Master)

Binning

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Automatic Exposure Control

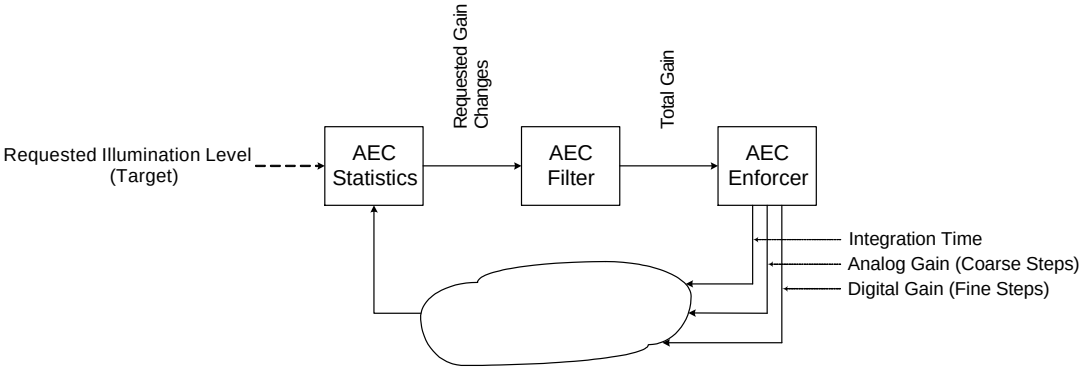

Figure 30. Automatic Exposure Control Loop

Target Illumination

desired_intensity

Table 14. AEC TARGET ILLUMINATION CONFIGURATION

Register

AEC Control Range

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AEC Update Frequency

Table 16. MINIMUM AND MAXIMUM EXPOSURE CONTROL PARAMETERS

Register	Name	Description
168[15:0]	min_exposure	Lower bound for the integration time applied by the AEC
169[1:0]	min_mux_gain	Lower bound for the first stage analog amplifier. This stage has three configurations with the following approximative gains: 0x0 = 1x 0x1 = 2x 0x2 = 4x
169[3:2]	min_afe_gain	Lower bound for the second stage analog amplifier. This stage has one configuration with the following approximative gain: 0x0 = 1.00x
169[15:4]	min_digital_gain	Lower bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format
170[15:0]	max_exposure	Upper bound for the integration time applied by the AEC
171[1:0]	max_mux_gain	Upper bound for the first stage analog amplifier. This stage has three configurations with the following approximative gains: 0x0 = 1x 0x1 = 2x 0x2 = 4x
171[3:2]	max_afe_gain	Upper bound for the second stage analog amplifier This stage has one configuration with the following approximative gain: 0x0 = 1.00x
171[15:4]	max_digit-al_gain	Upper bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format

gain_lat_comp

Exposure Control Status Registers

Table 17. EXPOSURE CONTROL STATUS REGISTERS

Register	Name	Description
Sequencer Status Registers		
242[15:0]	mult_timer	mult_timer for current frame (global shutter only). Note: this parameter is updated once it takes effect on the image.
243[15:0]	reset_length	Image array reset length for the current frame (global shutter only). Note: this parameter is updated once it takes effect on the image.
244[15:0]	exposure	Exposure for the current frame. Note: this parameter is updated once it takes effect on the image.
245[15:0]	exposure_ds	Dual slope exposure for the current frame. Note this parameter is not controlled by the AEC. Note: this parameter is updated once it takes effect on the image.
246[15:0]	exposure_ts	Triple slope exposure for the current frame. Note this parameter is not controlled by the AEC. Note: this parameter is updated once it takes effect on the image.
247[4:0]	mux_gainsw	1st stage analog gain for the current frame. Note: this parameter is updated once it takes effect on the image.
247[12:5]	afe_gain	2nd stage analog gain for the current frame. Note: this parameter is updated once it takes effect on the image.
248[11:0]	db_gain	Digital gain configuration for the current frame (5.7 unsigned format). Note: this parameter is updated once it takes effect on the image.
248[12]	dual_slope	Dual slope configuration for the current frame **Note 1**: this parameter is updated once it takes effect on the image. **Note 2**: This parameter is not controlled by the AEC.
248[13]	triple_slope	Triple slope configuration for the current frame. **Note 1**: this parameter is updated once it takes effect on the image. **Note 2**: This parameter is not controlled by the AEC.

Mode Changes and Frame Blanking

DATA OUTPUT FORMAT

Frame Format

P1−SN/SE/FN, P3−SN/SE/FN: LVDS Interface Version

LVDS Output Channels

8−bit / 10−bit Mode

Figure 31. P1−

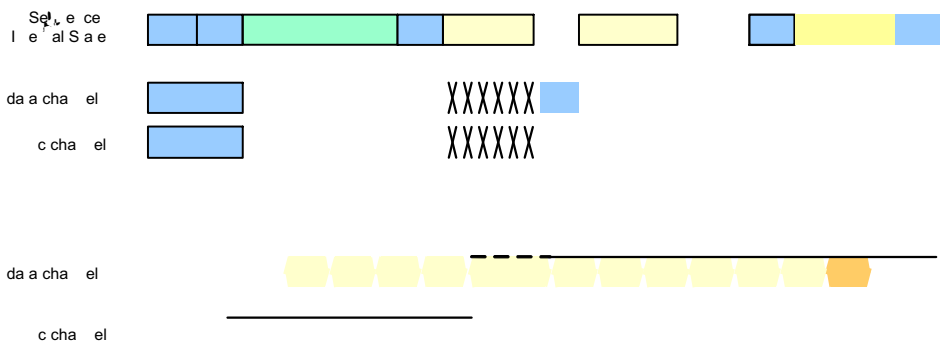

Figure 33. P1−SN/SE/FN, P3−SN/SE/FN: Time Line for Single Window Readout (at the start of a frame)

Data Order for P1−SN/SE/FN, P3−SN/SE/FN: LVDS Interface Version

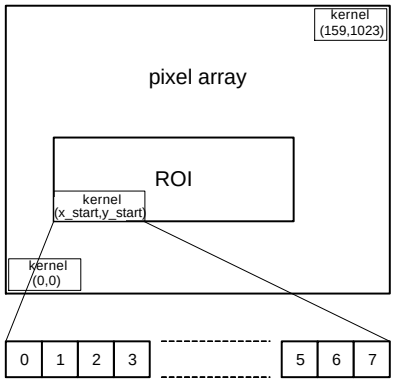

Figure 35. Kernel Organization in Pixel Array

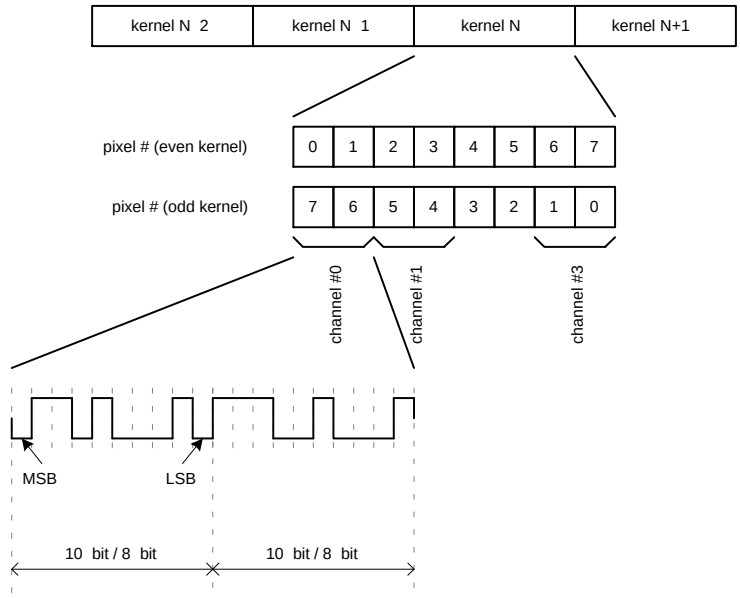

Figure 36. P1−SN/SE/FN: 4 LVDS Data Output Order when Subsampling is Disabled

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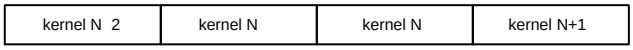

Figure 37. P1−SN/SE/FN, P3−SN/SE/FN: 2 LVDS Data Output Order when Subsampling is Disabled

♦

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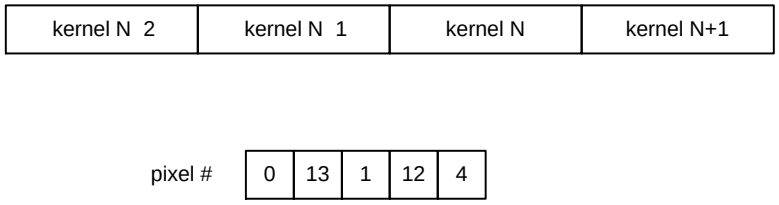

Figure 43. P1−SE, P3−SE: Data Output Order for 2 LVDS Output Channels in Subsampling Mode on a Color Sensor

P2−SN/SE: CMOS Interface Version

CMOS Output Signals

8−bit/10−bit Mode

Frame Format

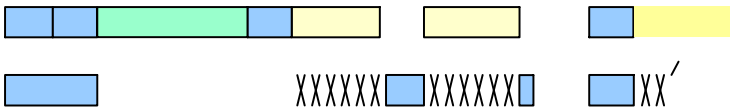

Figure 45. P2−SN/SE/FN: Frame Timing Indication

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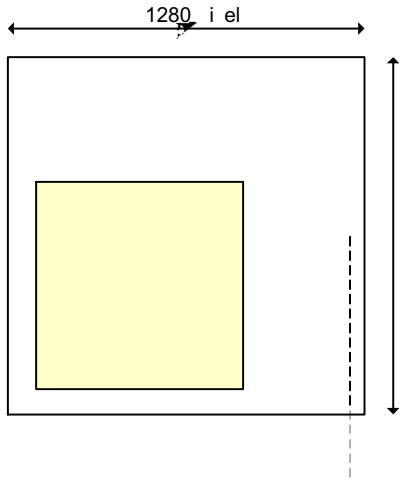

(a)

(b)

Figure 46. P2−SN/SE: Frame Format to Read Out Image Data

Data order for P2−SN/SE: CMOS Interface Version

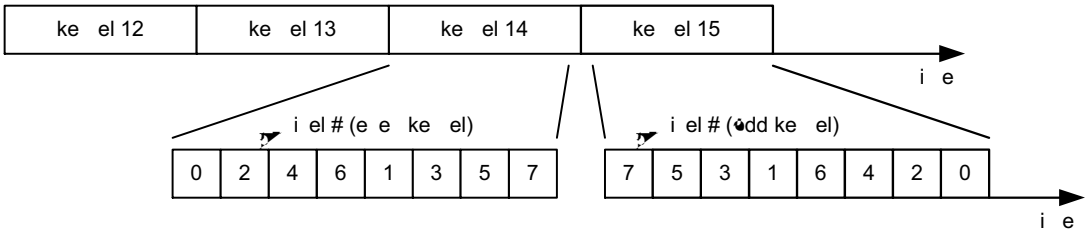

Figure 47. P2−SN/SE: Data Output Order without Subsampling

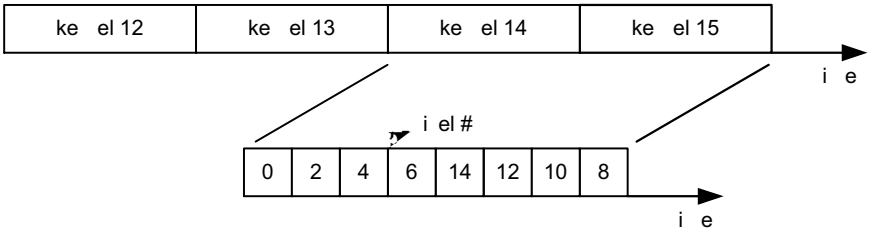

Figure 48. P2−SN: Data Output Order with Subsampling on a Monochrome Sensor

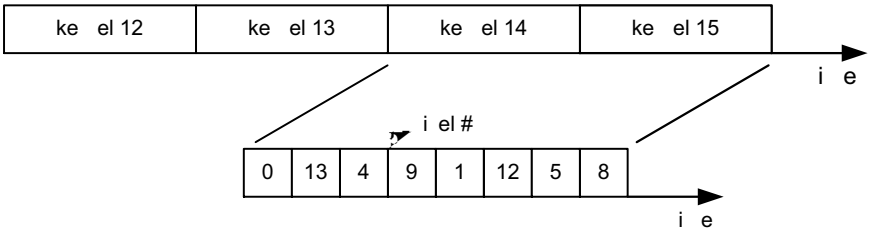

Figure 49. P2−SE: Data Output Order with Subsampling on a Color Sensor

Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
1	17		reserved	0x2113	8467	Reserved	RW
		[7:0]	reserved	0x13	19	Reserved	
		[12:8]	reserved	0x1	1	Reserved	
		[14:13]	reserved	0x1	1	Reserved	
I/O [Block Offset: 20]							
[redacted]	[redacted]	[redacted]	config1	0x0000	0	IO Configuration	RW
			clock_in_pwd_n	0x0	0	Power down Clock Input	
			reserved	0x0	0	Reserved	

Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[2]	colbias_enable	0x0	0	Bias Enable ‘0’: disabled ‘1’: enabled	
1	41		image_core_config1	0x0B5A	2906	Image Core Configuration	RW
		[3:0]	dac_ds	0xA	10	Double Slope Reset Level	
		[7:4]	dac_ts	0x5	5	Triple Slope Reset Level	
		[10:8]	reserved	0x3	3	Reserved	
		[12:11]	reserved	0x1	1	Reserved	
		[13]	reserved	0x0	0	Reserved	
		[14]					

Table 28. REGISTER MAP

Address Offset	Type

Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
6	118		sync_code1	0x0015	21	Data Formating - BL Indication	RW
		[9:0]	bl_0	0x015	21	Black Pixel Identification Sync Code - Even kernels	
7	119		sync_code2	0x0035	53	Data Formating - IMG Indication	RW
		[9:0]	img_0	0x035	53	Valid Pixel Identification Sync Code - Even kernels	
8	120		sync_code3	0x0025	37	Data Formating - IMG Indication	RW
		[9:0]	ref_0	0x025	37	Reference Pixel Identification Sync Code -	

Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default		Type
2	130			0x000F	15		RW
				0x1	1	Asser_valid for black lines when ‘1’, gate frame_valid for black lines when ‘0’. Parallel output mode only.	
				0x1	1	Assert line_valid for black lines when ‘1’, gate line_valid for black lines when ‘0’. Parallel output mode only.	
				0x1	1	Assert frame_valid for ref lines when ‘1’, gate frame_valid for black lines when ‘0’. Parallel output mode only.	
				0x1	1	Assert line_valid for ref lines when ‘1’, gate line_valid for black lines when ‘0’. Parallel output mode only.	
				0x0	0	Behaviour om3 29.707 ref357.449 594273.77 5667 .68033 53.7black lines when	

MAP

t Field	Register Name	Default (Hex)	Default	Description	Type
	test_configuration1	0x0302	770	Data Formating Test Configuration	RW
[7:0]	testpattern2_lsb	0x02	2	Testpattern used on datapath #2 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
15:8]	testpattern3_lsb	0x03	3	Testpattern used on datapath #3 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
	reserved	0x0504	1284	Reserved	RW
[7:0]	reserved	0x04	4	Reserved	
15:8]	reserved	0x05	5	Reserved	
	reserved	0x0706	1798	Reserved	RW
[7:0]	reserved	0x06	6	Reserved	
15:8]	reserved	0x07	7	Reserved	
	test_configuration16	0x0000	0	Data Formating Test Configuration	RW
[1:0]	testpattern0_msb	0x0	0	Testpattern used when testpattern_en = '1'	
[3:2]	testpattern1_msb	0x0	0	Testpattern used when testpattern_en = '1'	
[5:4]	testpattern2_msb	0x0	0	Testpattern used when testpattern_en = '1'	
[7:6]	testpattern3_msb	0x0	0	Testpattern used when testpattern_en = '1'	
[9:8]	reserved	0x0	0	Reserved	
1:10]	reserved	0x0	0	Reserved	
3:12]	reserved	0x0	0	Reserved	
5:14]	reserved	0x0	0	Reserved	
	reserved	0x0000	0	Reserved	RW
15:0]	reserved	0x0000	0	Reserved	
	reserved	0x0000	0	Reserved	RW
15:0]	reserved	0x0000	0	Reserved	

	configuration	0x0010	16	AEC Configuration	RW
[0]	enable	0x0	0	AEC Enable	
[1]	restart_filter	0x0	0	Restart AEC filter	
[2]	freeze	0x0	0	Freeze AEC filter and enforcer gains	
[3]	pixel_valid	0x0	0	Use every pixel from channel when 0, every 4th pixel when 1	
[4]	amp_pri	0x1	1	Column amplifier gets higher priority than AFE PGA in gain distribution if 1. Vice versa if 0	
	intensity	0x60B8			

Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
20	180		reserved	0x0100	256	Reserved	RW

Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[15]	reserved	0x0	0	Reserved	
1	193						

Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[12:8]	gate_first_line	0x1	1	Blank out first lines 0: no blank 1-31: blank 1-31 lines	
6	198		reserved	0x0000	0	Reserved	RW
		[11:0]	reserved	0x000	0	Reserved	
7	199		mult_timer0	0x0001	1	Exposure/Frame Rate Configuration	RW

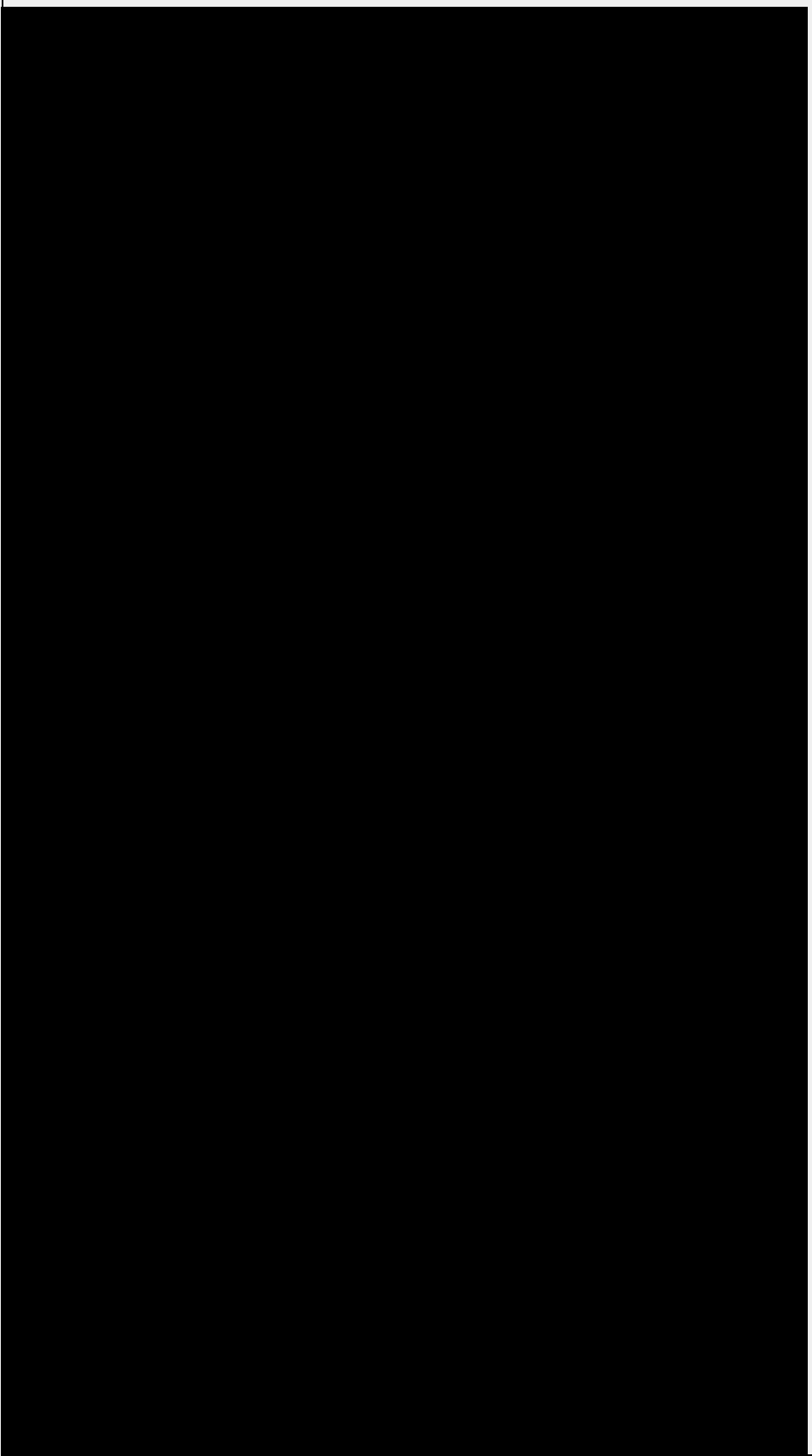

Table 28. REGISTER MAP

Address Offset	Default (Hex)	Default	Description	Type

Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
4	260		roi1_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
5	261		roi1_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
6	262		roi2_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
7	263		roi2_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
8	264		roi2_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
9	265		roi3_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
10	266		roi3_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
11	267		roi3_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
12	268		roi4_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
13	269		roi4_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
14	270		roi4_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
15	271		roi5_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
16	272		roi5_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
17	273		roi5_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
18	274		roi6_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
19	275		roi6_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
20	276		roi6_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	
21	277		roi7_configuration0	0x9F00	40704	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0x9F	159	X End Configuration	
22	278		roi7_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	

Table 28. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
23	279		roi7_configuration2	0x03FF	1023	ROI Configuration	RW
		[12:0]	y_end	0x3FF	1023	Y End Configuration	

Sequencer ROI [Block Offset: 384]

0	384		reserved			Reserved	RW
		[15:0]	reserved			Reserved	
	..	…	…			…	
			…			…	
127	511		reserved			Reserved	RW
		[15:0]	reserved			Reserved	

PACKAGE INFORMATION

Pin List

Table 29. PIN LIST FOR P1−SN/SE/FN, P3−SN/SE/FN LVDS INTERFACE

Pack Pin No.	Pin Name	I/O Type	Direction	Description
1	vdd_33	Supply		3.3 V Supply
2	mosi	CMOS	Input	SPI Master Out Slave In
3	miso	CMOS	Output	SPI Master In Slave Out
4	sck	CMOS	Input	SPI Clock
5	gnd_18	Supply		1.8 V Ground
6	vdd_18	Supply		1.8 V Supply
7	clock_outn	LVDS	Output	LVDS Clock Output (Negative)
8	clock_outp	LVDS	Output	LVDS Clock Output (Positive)
9	doutn0	LVDS	Output	LVDS Data Output Channel #0 (Negative)
10	doutp0	LVDS	Output	LVDS Data Output Channel #0 (Positive)
11	doutn1	LVDS	Output	LVDS Data Output Channel #1 (Negative). Not connected for P3
12	doutp1	LVDS	Output	LVDS Data Output Channel #1 (Positive). Not connected for P3
13	doutn2	LVDS	Output	LVDS Data Output Channel #2 (Negative)
14				

Table 29. PIN LIST FOR P1−SN/SE/FN, P3−SN/SE/FN LVDS INTERFACE

Pack Pin No.	Pin Name	I/O Type	Direction	Description
36				

Table 30. PIN LIST FOR P2−SN/SE CMOS INTERFACE

Pack Pin No.	Pin Name	I/O Type	Direction	Description
26	vdd_18	Supply		1.8 V Supply
27	gnd_18	Supply		1.8 V Ground
28	ibias_master	Analog	I/O	

Table 31. MECHANICAL SPECIFICATION

Parameter	Description	Min	Typ	Max	Units
Die (Refer to Figure 51 and Figure 52 showing Pin 1 reference as left center)	Die thickness		725		μm
	Die Size		9.0 X 7.95		mm^2
	Die center, X offset to the center of package	50	0	50	μm
	Die center, Y offset to the center of the package	225	175	125	μm
	Die position, tilt to the Die Attach Plane	1	0	1	deg
	Die rotation accuracy (referenced to die scribe and lead fingers on package on all four sides)	1	0	1	deg
	Optical center referenced from the die/package center (X dir)		179.24		μm
	Optical center referenced from the die center (Y dir)		1542.14		μm
	Optical center referenced from the package center (Y dir)		1367.14		μm
	Distance from bottom of the package to top of the die surface	1.165	1.260	1.405	mm
	Distance from top of the die surface to top of the glass lid	0.655	0.990	1.305	mm
Glass Lid Specification	XY size		13.6 X 13.6		mm^2
	Thickness	0.5	0.55	0.6	mm
	Spectral response range	400		1000	nm

Package Drawing

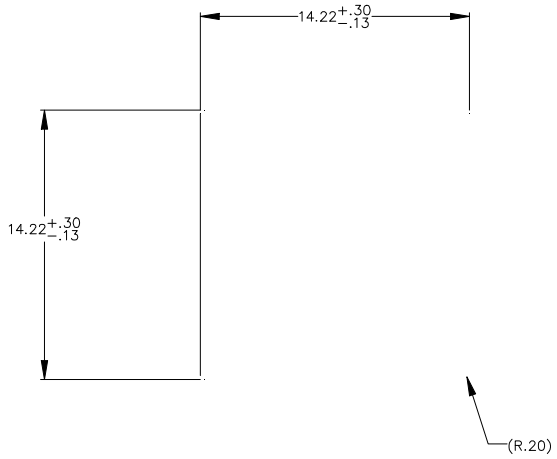

Figure 50. Package Drawing for the 48−pin LCC Package

Table 32. OPTICAL CENTER INFORMATION

		PYTHON1300		PYTHON500		PYTHON300	
	References*	**X (μm)**	**Y (μm)**	**X (μm)**	**Y (μm)**	**X (μm)**	**Y (μm)**
Die Outer Cordinates	D1	0	9000	0	9000	0	9000
	D2	7950	9000	7950	9000	7950	9000
	D3	7950	0	7950	0	7950	0
	D4	0	0	0	0	0	0
Die Center	CD	3975	4500	3975	4500	3975	4500
Pixel Area Coordinates	A1	704.56	8518.94	704.56	8518.94	704.569000	

Packing and Tray Specification

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Table 33. PACKING AND TRAY SPECIFICATION

CLCC	Package (mm)			Tray	Restraint	Box
Leads	Length	Width	Thickness*			

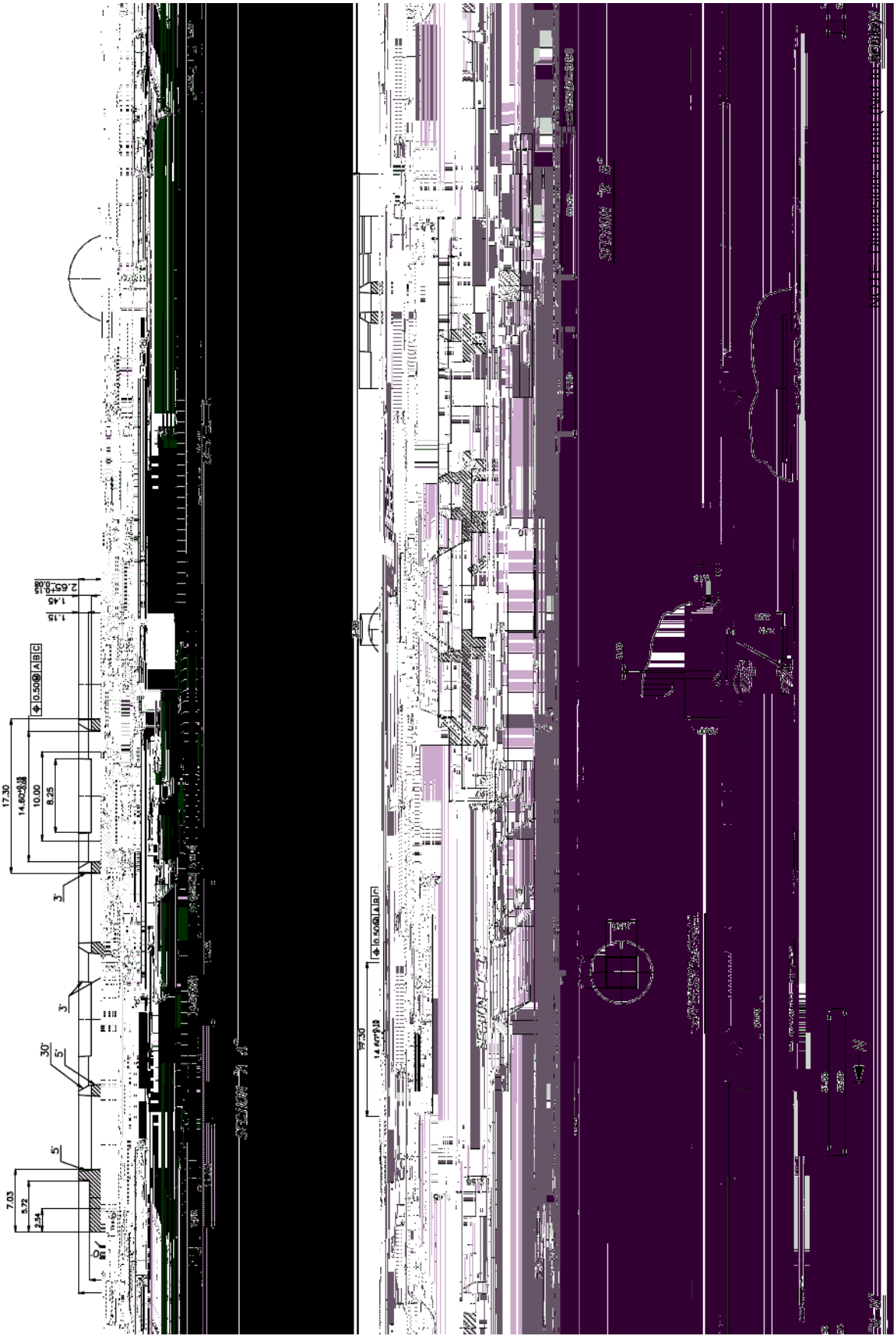

Figure 54. Packing and Tray Configuration (2 of 2)

Glass Lid

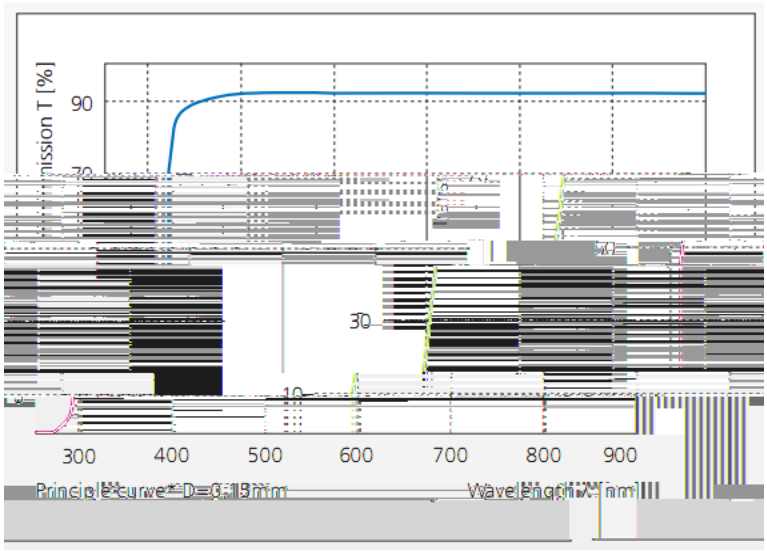

Figure 55. Transmission Characteristics of the Glass Lid

Protective Foil

(units in mm)

Figure 56. Dimensions of the Protective Foil

onsemi *Quality & Reliability*

Useful References

Image Sensor Handling and Best Practices