

Silicon Carbide (SiC) MOSFET - EliteSiC, 32 mohm, 650 V, M3S, D2PAK-7L

NTBG032N065M3S

- Typical $R_{DS(ON)} = 32 \text{ m}\Omega$ @ $V_{GS} = 18 \text{ V}$
- Ultra Low Gate Charge (Q_{G(tot)} = 55 nC)
- High Speed Switching with Low Capacitance (Coss = 113 pF)
- 100% Avalanche Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb–Free 2LI (on Second Level Interconnection)
- SMPS, Solar Inverters, UPS, Energy Storages, EV charging infrastructure

 $(T_J = 25^{\circ}C \text{ unless otherwise noted})$

Drain-to-Source Voltage	V_{DSS}	650	V
Gate-to-Source Voltage	V_{GS}	-8/+22	

μS

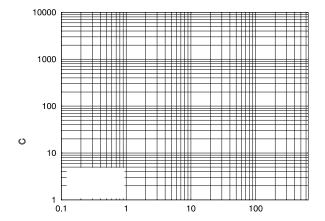
		I _{DM}	156	Α
Continuous Source-Drain Current (Body Diode)	$T_C = 25$ °C, $V_{GS} = -3$ V	I _S	30	
	$T_{C} = 100^{\circ}C,$ $V_{GS} = -3 \text{ V}$		17	
Pulsed Source–Drain Current (Body Diode) (Note 1)	$T_{C} = 25^{\circ}C,$ $V_{GS} = -3 \text{ V},$ $t_{P} = 100 \mu\text{s}$	I _{SM}	127	
Single Pulse Avalanche Energy (Note 2)	I _{LPK} = 16.7 A, L = 1 mH	E _{AS}		

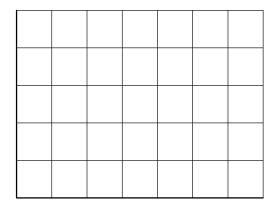


 $(T_J = 25^{\circ}C \text{ unless otherwise specified})$ (continued)

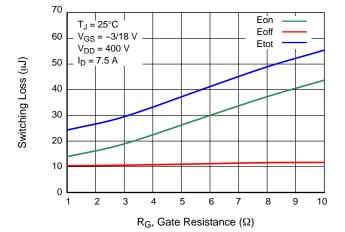
	<u>.</u>	1		
Turn-On Delay Time	t _d (ON)	$V_{GS} = -3/18 \text{ V}, I_D = 15 \text{ A}, V_{DD}$		

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D²PAK7 (TO-263-7L HV) CASE 418BJ ISSUE B

DATE 16 AUG 2019

Α

c2

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C

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code

A = Assembly Location

Y = Year WW = Work Week G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

