July, 2024

ELECTRICAL CHARACTERISTICS (continued)
T_J = 25 °C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Total Gate Charge	V_{DS} = 800 V, V_{GS} = −3/18 V, I_D = 60 A	$Q_{G(TOTAL)}$	−	211	−	nC
Gate−Source Charge		Q_{GS}	−	16	−	nC
Gate−Drain Charge		Q_{GD}	−	50	−	nC
Turn−on Delay Time	T_J = 25°C V_{DS}= 800 V, I_D = 60 A V_{GS} = −3 V / 18 V, R_G = 2.7 Ω	$t_{d(on)}$	−	25	−	ns
Rise Time		t_r	−	9	−	
Turn−off Delay Time		$t_{d(off)}$	−	94	−	
Fall Time		t_f	−	8	−	
Turn−on Switching Loss per Pulse		E_{ON}	−	1190	−	μJ
Turn−off Switching Loss per Pulse		E_{OFF}	−	120	−	
Turn−on Delay Time	T_J = 150°C V_{DS}= 800 V, I_D = 60 A V_{GS} = −3 V / 18 V, R_G = 2.7 Ω	$t_{d(on)}$	−	22	−	ns
Rise Time		t_r	−	10	−	
Turn−off Delay Time		$t_{d(off)}$	−	107	−	
Fall Time		t_f	−	8	−	
Turn−on Switching Loss per Pulse		E_{ON}	−	1560	−	μJ
Turn−off Switching Loss per Pulse		E_{OFF}	−	170	−	
Diode Forward Voltage	V_{GS} = −3 V, I_{SD} = 60 A, T_J = 25°C	VSD	−	4.67	6.2	V
	V_{GS} = −3 V, I_{SD} = 60 A, T_J = 125°C		−	4.45	−	
	V_{GS} = −3 V, I_{SD} = 60 A, T_J = 150°C		−	4.4	−	
Thermal Resistance − Chip−to−Case	M1, M2	R_{thJC}	−	0.48	−	°C/W
Thermal Resitance −						

TYPICAL CHARACTERISTICS

M1/M2 SIC MOSFET CHARACTERISTIC

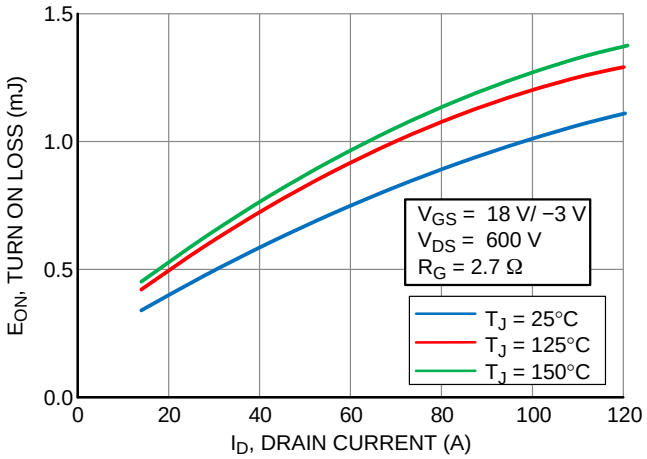


Figure 8. Switching On Loss vs. Drain Current V_{DS} = 600 V

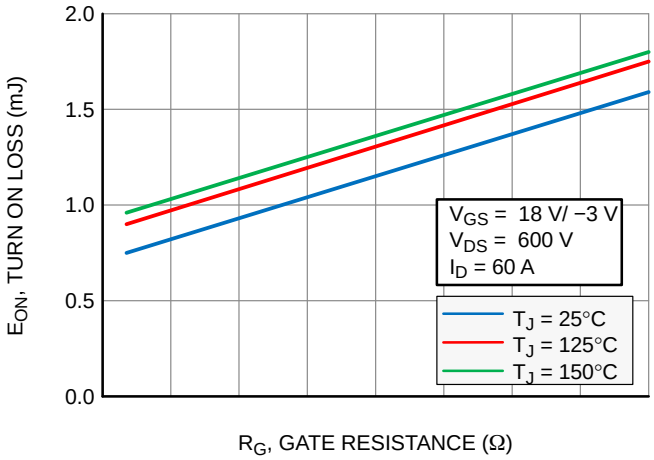


Figure 9. Switching On Loss vs. Gate Resistance V_{DS} = 600 V

TYPICAL CHARACTERISTICS

M1/M2 SIC MOSFET CHARACTERISTIC

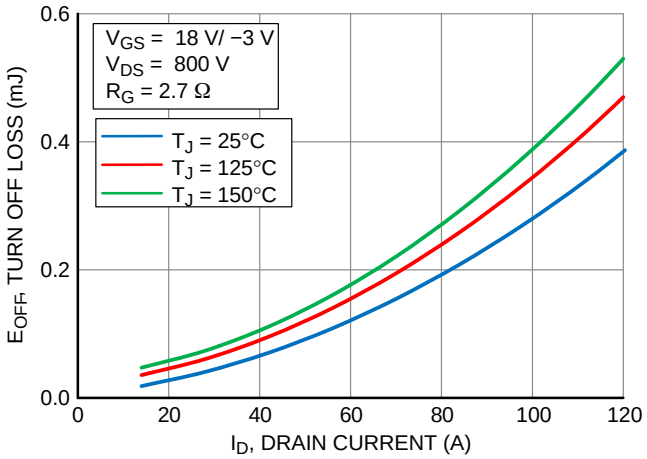


Figure 14. Switching Off Loss vs. Drain Current V_{DS} = 800 V

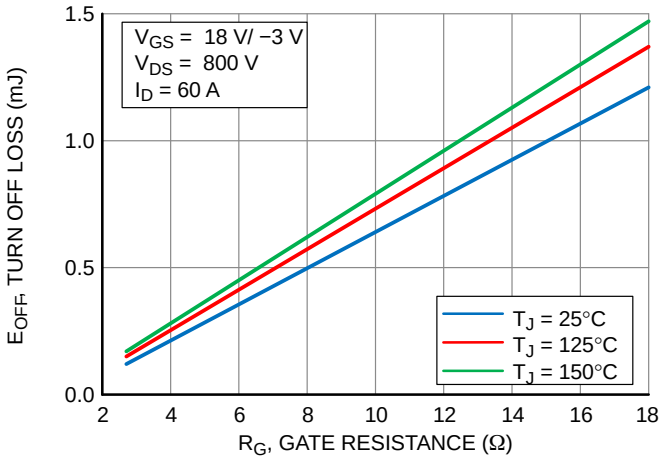
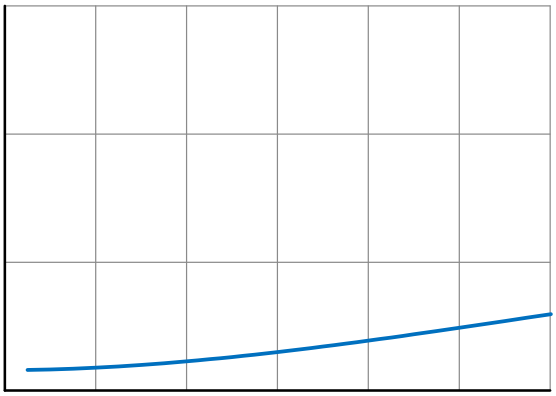
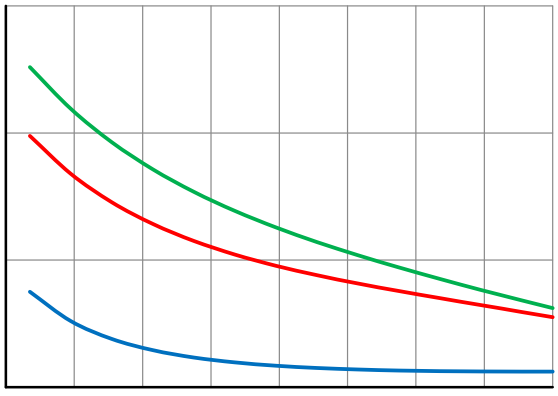


Figure 15. Switching Off Loss vs. Gate Resistance V_{DS} = 800 V





TYPICAL CHARACTERISTICS

M1/M2 SIC MOSFET CHARACTERISTIC

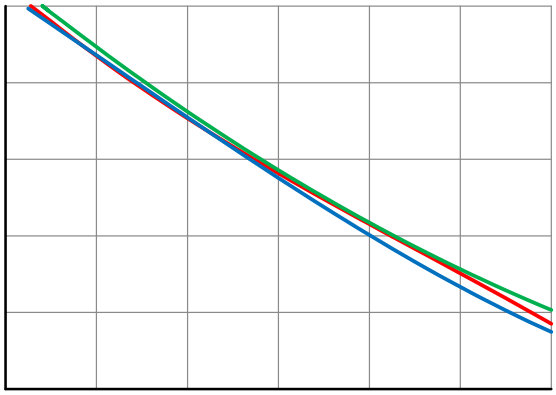


Figure 20. di/dt Turn Off vs. Drain Current
V_{DS} = 800 V

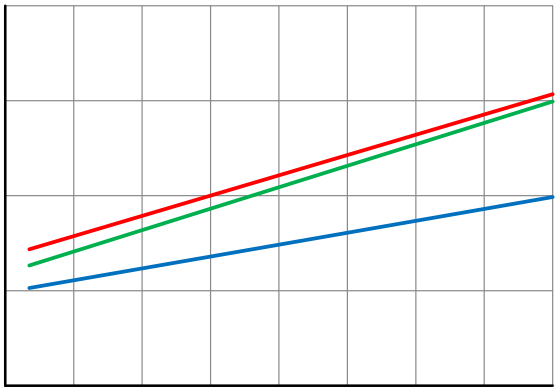


Figure 21. di/dt Turn Off vs. Gate Resistance
V_{DS} = 800 V

TYPICAL CHARACTERISTICS

M1/M2 SIC MOSFET CHARACTERISTIC

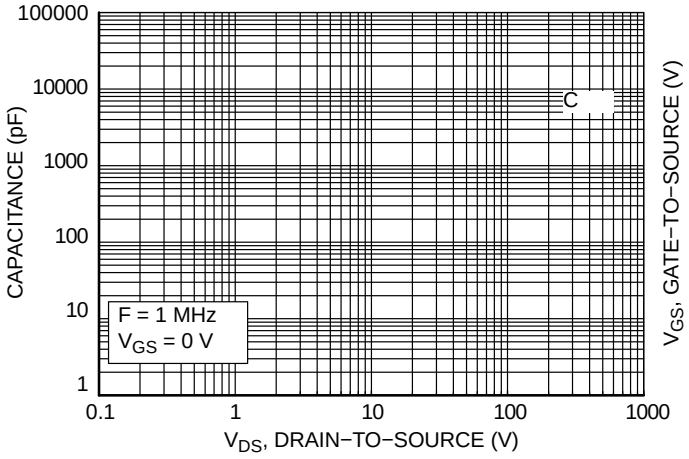


Figure 26. Capacitance vs. Drain−to−Source Voltage

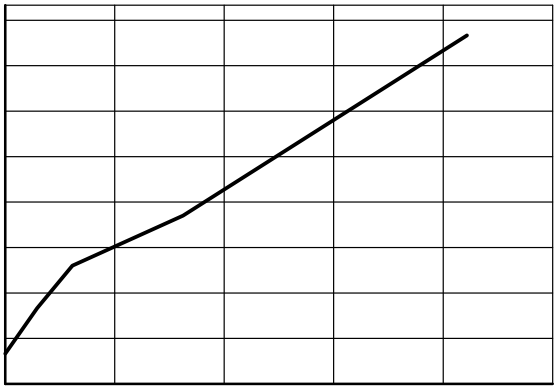


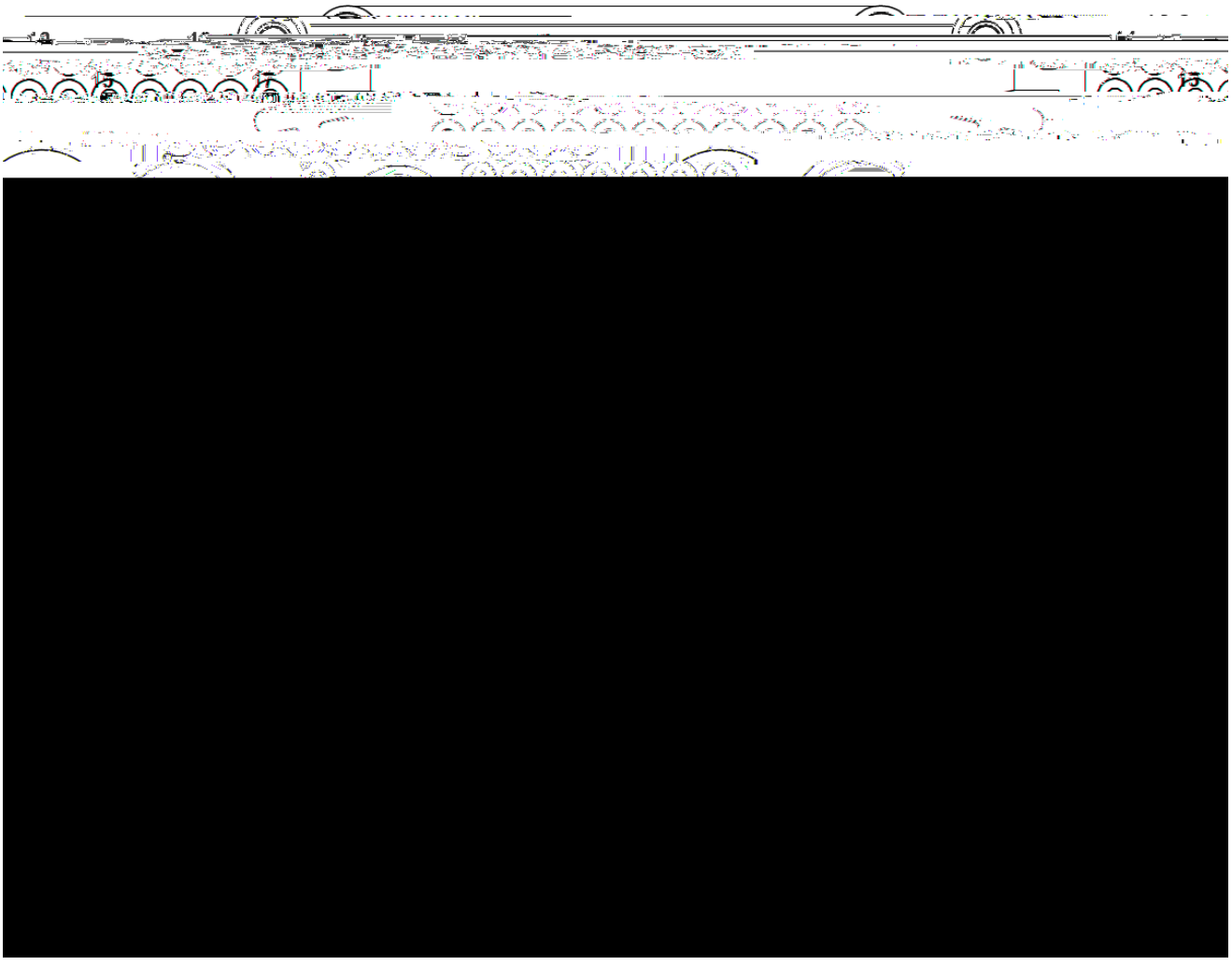
Figure 27. Gate−to−Source Voltage vs. Gate Charge

Table 1. CAUER NETWORKS

Cauer Element #	Rth (K/W)	Cth (Ws/K)
1	0.0004413	0.0013801
2	0.0029539	0.0003074
3	0.0066160	0.0005317
4	0.0326540	0.0026575
5	0.0988730	0.0081213
6	0.1850100	0.0419900
7	0.0817340	1.1620000

PIN POSITION INFORMATION

scale = 2.5 : 1



PIM18 33.8x42.5 (PRESS FIT)
CASE 180BW
ISSUE B

DATE 30 APR 2021

GENERIC
MARKING DIAGRAM*