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Description

The PCA9554 is a CMOS device that provides 8−bit parallel input/output port expansion for I^2C and SMBus compatible applications. This I/O expander provides a simple solution in applications where additional I/Os are needed: sensors, power switches, LEDs, pushbuttons, and fans.

The PCA9554 consist of an input port register, an output port

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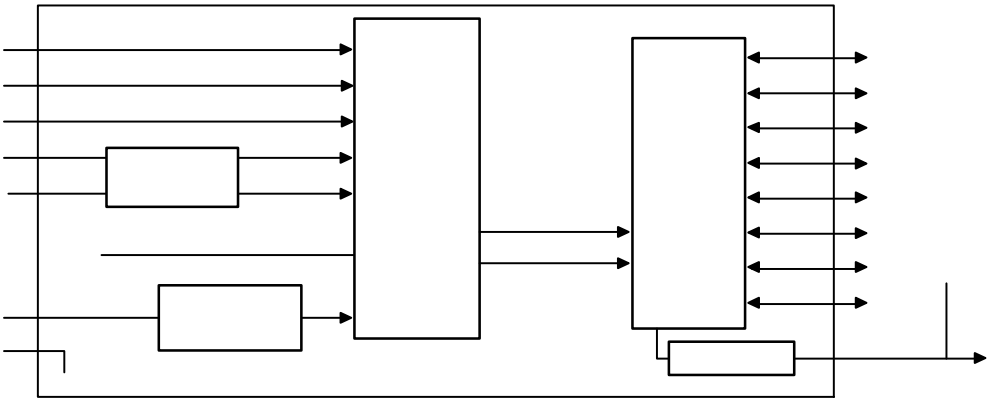


Figure 1. Block Diagram

Table 4. D.C. OPERATING CHARACTERISTICS (V_{CC} = 2.3 to 5.5 V; T_A = −40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLIES						
V_{CC}	Supply voltage		2.3	−	5.5	V
I_{CC}	Supply current	Operating mode; V_{CC} = 5.5 V; no load; f_{SCL} = 100 kHz	−	104	175	μA
I_{stbl}	Standby current	Standby mode; V_{CC} = 5.5 V; no load; V_I = V_{SS}; f_{SCL} = 0 kHz; I/O = inputs	−	550	700	μA
I_{stbh}	Standby current	Standby mode; V_{CC} = 5.5 V; no load; V_I = V_{CC}; f_{SCL} = 0 kHz; I/O = inputs	−	0.25	1	μA
V_{POR}	Power−on reset voltage	No load; V_I = V_{CC} or V_{SS}	−	1.5	1.65	V
SCL, SDA, $\overline{INT}$						
V						

Table 5. A.C. CHARACTERISTICS (V_{CC} = 2.3 V to 5.5 V; T_A = −40°C to +85°C, unless otherwise specified.) (Note 8)

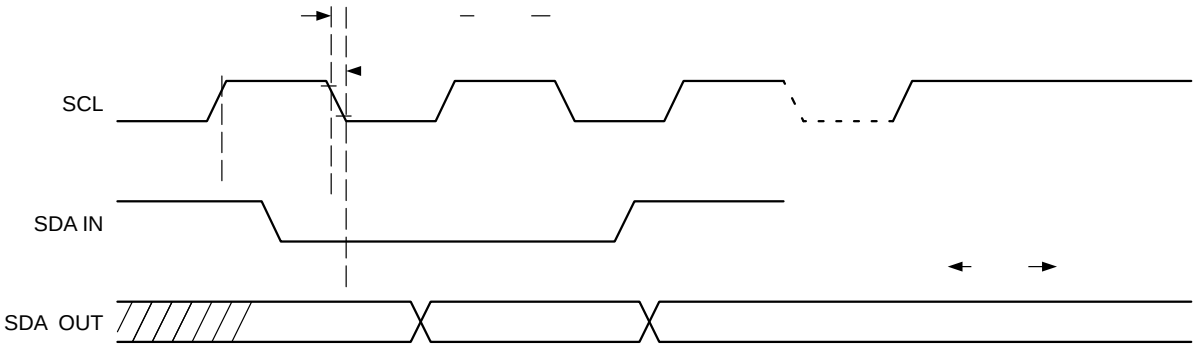
Symbol	Parameter	Standard I^2C		Fast I^2C		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R (Note 9)	SDA and SCL Rise Time		1000		300	ns
t_F (Note 9)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF} (Note 9)	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		50		ns
T_i (Note 9)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns

Symbol	Parameter	Min	Max	Units
PORT TIMING				
t_{PV}	Output Data Valid		200	ns
t_{PS}	Input Data Setup Time	100		ns
t_{PH}	Input Data Hold Time	1		μs
INTERRUPT TIMING				
t_{IV}	Interrupt Valid		4	μs
t_{IR}	Interrupt Reset		4	μs

8. Test conditions according to “AC Test Conditions” table.
9. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

Table 6. A.C. TEST CONDITIONS

Input Rise and Fall time	≤ 10 ns
CMOS Input Voltages	0.2 V_{CC} to 0.8 V_{CC}
CMOS Input Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}
TTL Input Voltages	0.4 V to 2.4 V
TTL Input Reference Voltages	0.8 V, 2.0 V
Output Reference Voltages	0.5 V_{CC}
Output Load: SDA, $\overline{INT}$	Current Source I_{OL} = 3 mA; C_L = 100 pF
Output Load: I/Os	Current Source: I_{OL}/I_{OH} = 10 mA; C_L = 50 pF


SCL
SDA IN
SDA OUT

Functional Description

The PCA9554's general purpose input/output (GPIO) peripherals provide up to eight I/O ports, controlled through an I^2C compatible serial interface.

The PCA9554 supports the I^2C Bus data transmission protocol. This I^2C Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The PCA9554 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 6).

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The PCA9554 monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 6).

The PCA9554 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8−bit byte.

When the PCA9554 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the PCA9554 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a STOP condition to return the PCA9554 to the standby power mode and place the device in a known state.

Registers and Bus Transactions

The PCA9554 consists of an input port register, an output port register, a polarity inversion register and a configuration register. Table 7 shows the register address table. Tables 8 to 11 list Register 0 through Register 3 information.

Table 7. REGISTER COMMAND BYTE

Command (hex)	Protocol	Function
0x00	Read byte	Input port register
0x01	Read/write byte	Output port register
0x02	Read/write byte	Polarity inversion register
0x03	Read/write byte	Configuration register

The command byte is the first byte to follow the device address byte during a write/read bus transaction. The register command byte acts as a pointer to determine which register will be written or read.

The input port register is a read only port. It reflects the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output by the configuration register. Writes to the input port register are ignored.

Table 8. REGISTER 0 – INPUT PORT REGISTER

bit	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
default	1	1	1	1	1	1	1	1

Table 9. REGISTER 1 – OUTPUT PORT REGISTER

bit	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
default	1	1	1	1				

The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Bit values in this register have no effect on I/O pins defined as inputs. Reads from the output port register reflect the value that is in the flip−flop controlling the output, not the actual I/O pin value.

The polarity inversion register allows the user to invert the polarity of the input port register data. If a bit in this register is set (“1”) the corresponding input port data is inverted. If a bit in the polarity inversion register is cleared (“0”), the original input port polarity is retained.

The configuration register sets the directions of the ports. Set the bit in the configuration register to enable the corresponding port pin as an input with a high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At power−up, the I/Os are configured as inputs with a weak pull−up resistor to V_{CC}.

Data is transmitted to the PCA9554’s registers using the write mode shown in Figure 9 and Figure 10.

The PCA9554’s registers are read according to the timing diagrams shown in Figure 11 and Figure 12. Once a command byte has been sent, the register which was addressed will

Power−On Reset Operation

When the power supply is applied to V_{CC} pin, an internal power−on reset pulse holds the PCA9554 in a reset state until V_{CC} reaches V_{POR} level. At this point, the reset condition is released and the internal state machine and the PCA9554's registers are initialized to their default state.

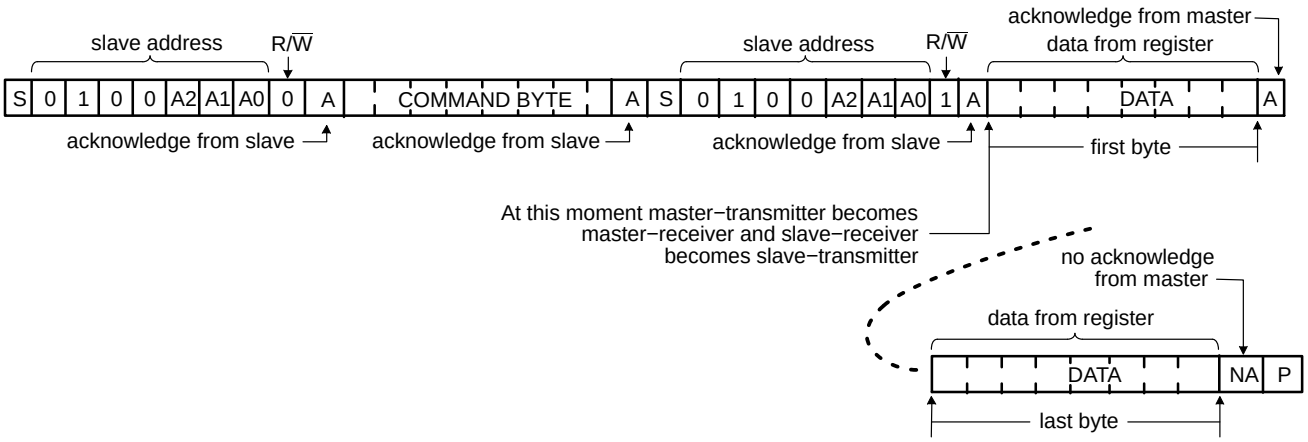


Figure 11. Read from Register

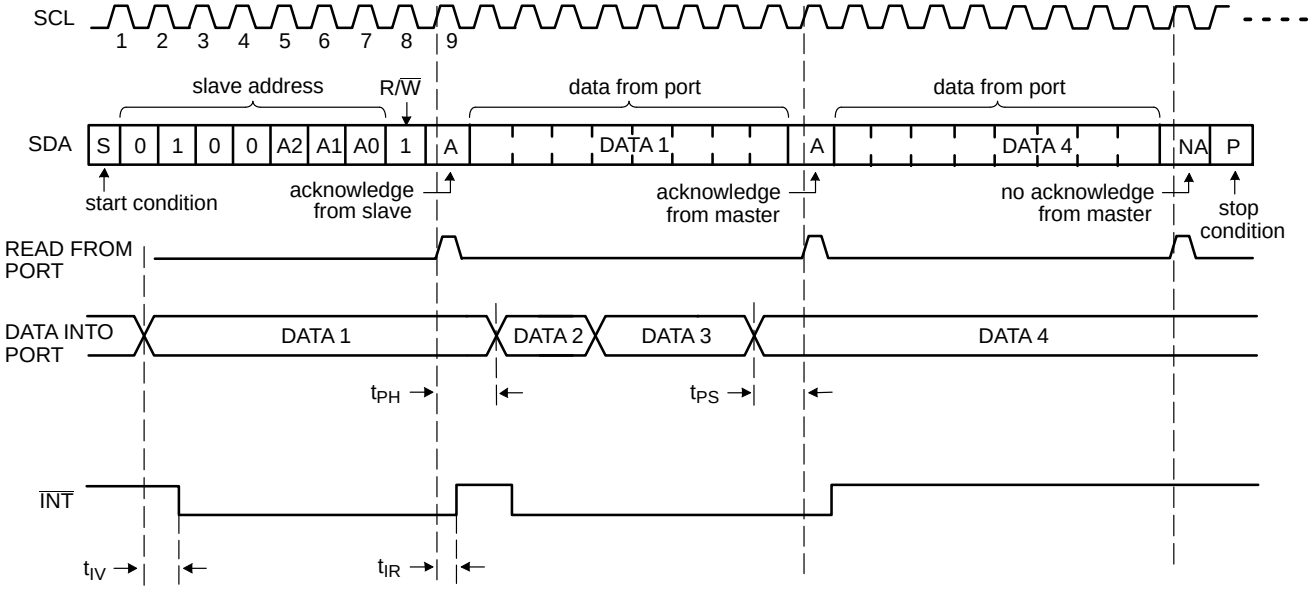


Figure 12. Read Input Port Register

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