FEATURES

- **Arm Cortex−M3 Processor:** − −
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RSL10 INTERNAL BLOCK DIAGRAM

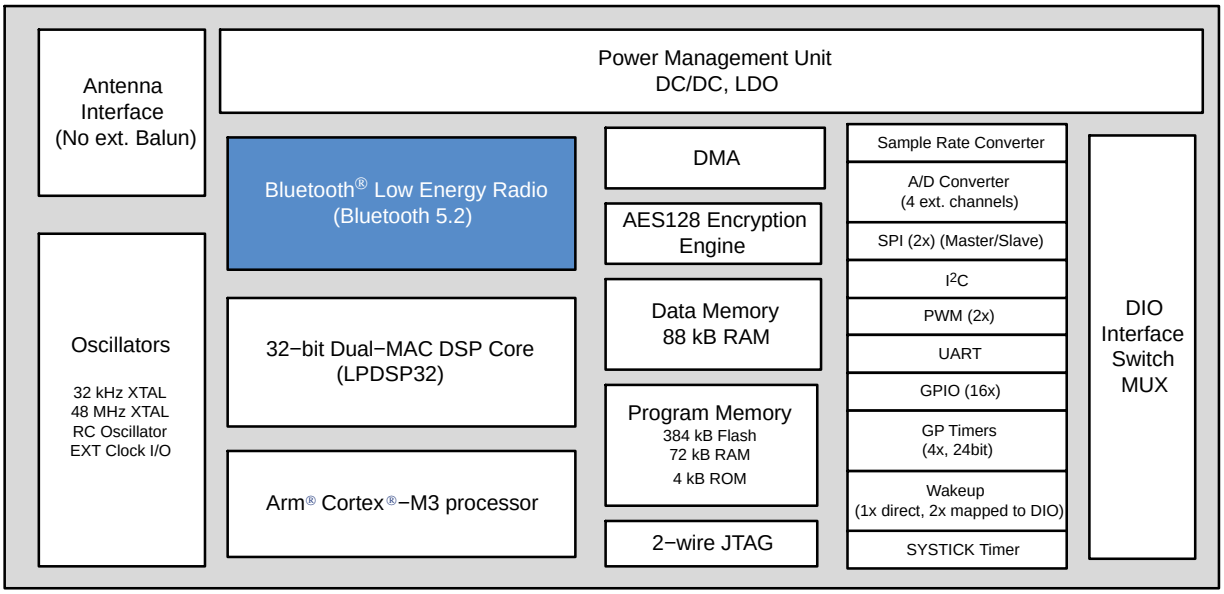

Figure 1. RSL10 Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VBAT	Power Suppl0Ryoltage		3.63	V
VDDO	I/O Suppl0Ryoltage (Note 1)		3.63	V

Table 2. RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage Operating Range	VBAT	Input supply voltage on VBAT pin (Note 4)	1.18	1.25	3.3	V
Functional Temperature Range	T functional		−40	−	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. In order to be able to use a VBAT Min of 1.1 V, the following reduced operating conditions should be observed:
   − Maximum Tx power 0 dBm.
   − SYSCLK ≤ 24 MHz.
   − Functional temperature range limited to 0−50°C
   The following trimming parameters should be used:
   − VCC = 1.10 V
   − VDDC = 0.92 V
   − VDDM = 1.05 V, will be limited by VCC at end of battery life
   − VDDRF = 1.05 V, will be limited by VCC at end of battery life. VDDPA should be disabled
   RSL10 should enter in end−of−battery−life operating mode if VCC falls below 1.03 V. VCC will remain above 1.03 V if VBAT ≥ 1.10 V under the restricted operating conditions described above.

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Unit
OVERALL						
Current consumption RX, V_{BAT} = 1.25 V, low latency	I_{VBAT}	RX Mode, **onsemi** proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay.		1.8		mA
Current consumption TX, V_{BAT} = 1.25 V, low latency	I_{VBAT}	TX Mode, **onsemi** proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay. Transmit power: 0 dBm		1.8		mA
Current consumption RX, V_{BAT} = 1.25 V	I_{VBAT}	RX Mode, **onsemi** proprietary audio streaming protocol at 7 kHz audio BW, 37 ms delay.		1.15		mA
Deep sleep current, example 1, V_{BAT} = 1.25 V	Ids1	Wake up from wake up pin or DIO wake up.		50		nA
Deep sleep current, example 2, V_{BAT} = 1.25 V	Ids2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.		90		nA
Deep sleep current, example 3, V_{BAT} = 1.25 V	Ids3	As Ids2 but with 8 kB RAM data retention.		300		nA
Standby Mode current, V_{BAT} = 1.25 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.		30		μA
Current consumption RX, V_{BAT} = 3 V	I_{VBAT}	RX Mode, **onsemi** proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay.		0.9		mA
Current consumption TX, V_{BAT} = 3 V	I_{VBAT}	TX Mode, **onsemi** proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay. Transmit power: 0 dBm		0.9		mA
Deep sleep current, example 1, V_{BAT} = 3 V	Ids1	Wake up from wake up pin or DIO wake up.		25		nA
Deep sleep current, example 2, V_{BAT} = 3 V	Ids2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.		40		nA
Deep sleep current, example 3, V_{BAT} = 3 V	Ids3	As Ids2 but with 8 kB RAM data retention.		100		nA
Standby Mode current, V_{BAT} = 3 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.		17		μA

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Unit
EEMBC ULPMark BENCHMARK, CORE PROFILE						
ULPMark CP 3.0 V		Arm Cortex−M3 processor running from RAM, VBAT= 3.0 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1090		ULP Mark
ULPMark CP 2.1 V		Arm Cortex−M3 processor running from RAM, VBAT= 2.1 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1260		ULP Mark
EEMBC CoreMark BENCHMARK for the Arm Cortex−M3 Processor and the LPDSP32 DSP						
Arm Cortex−M3 processor running from RAM		At 48 MHz SYSCLK. Using the IAR 8.10.1 C compiler, certified		159		Core Mark
LPDSP32 running from RAM		At 48 MHz SYSCLK Using the 2020.03 release of the Synopsys LPDSP32 C compiler		174		Core Mark
Arm Cortex−M3 processor and LPDSP32 running from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK		123		Core Mark/ mA
Arm Cortex−M3 processor and LPDSP32 running from RAM, VBAT = 3 V		At 48 MHz SYSCLK		293		Core Mark/ mA
Arm Cortex−M3 processor running CoreMark from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK (processor consumption only)		29.1		µA/MHz
Arm Cortex−M3 processor running CoreMark from RAM, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		12.3		µA/MHz
Arm Cortex−M3 processor running CoreMark from Flash, VBAT = 1.25 V		At 48 MHz SYSCLK (processor consumption only)		34.3		µA/MHz
Arm Cortex−M3 processor running CoreMark from Flash, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		14.6		µA/MHz
LPDSP32 running CoreMark from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK (processor consumption only)		19.5		µA/MHz
LPDSP32 running CoreMark from RAM, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		8.2		µA/MHz
INTERNALLY GENERATED VDDC: Digital Block Supply Voltage						
Supply voltage: operating range	VDDC		0.92	1.15	1.32 (Note 5)	

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Unit
INTERNALLY GENERATED VDDPA: Optional Radio Power Amplifier Supply Voltage						

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Unit
ADC						
Resolution	ADC_{RES}		8	12	14	bits
Input voltage range	ADC_{RANGE}		0		2	V
INL	ADC_{INL}		−2		+2	mV
DNL	ADC_{DNL}		−1		+1	mV
Channel sampling frequency	ADC_{CH_SF}	For the 8 channels sequentially, SLOWCLK = 1 MHz	0.0195		6.25	kHz
32 kHz ON−CHIP RC OSCILLATOR						
Untrimmed Frequency	$Freq_{UNTR}$		20	32	50	kHz
Trimming steps	Steps			1.5		%
3 MHz ON−CHIP RC OSCILLATOR						
Untrimmed Frequency	$Freq_{UNTR}$		2	3	5	MHz
Trimming steps	Steps			1.5		%
Hi Speed mode	Fhi			10		MHz
32 kHz ON−CHIP CRYSTAL OSCILLATOR						

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Unit
FLASH SPECIFICATIONS						
Endurance for sections NVR1, NVR2, and NVR3 (6 kB in total)			1000			write/ erase cycles
Retention			25			years

Table 8. BUMP AND COATING SPECIFICATIONS

Subject	Specification
Bump metallization	Sn 97.7%/Ag 2.3%
Backside coating specification	

Table 9. CHIP INTERFACE SPECIFICATIONS

Pad Name	Description	Power Domain	I/O	A/D	Pull	Pad #, WLCSP	Pad #, QFN48
VBAT	Battery input voltage	VBAT	I	P		K5,K7,K10	9
VDC	DC−DC output voltage to external LC filter		O	A		J11	10
VCC	DC−DC filtered output		I	P/A		K11	12
XTAL32_IN	Xtal input pin for 32 kHz xtal		I/O	A		L10	14
XTAL32_OUT	Xtal output pin for 32 kHz xtal		I/O	A		L11	13
VSSA	Analog ground		I/O	P		E10	8
RES	RESERVED		I	D	D	F8	11
VDDA	Charge pump output for analog and flash supplies	VDDA	I/O	P/A		F11	5
VDDRF	LDO's output for radio voltage supply		I/O	P/A		A11	48
CAP0	Pump capacitor connection		O	A		H11	7
CAP1	Pump capacitor connection		O	A		G10	6
AOUT	Analog test pin		O	A		L6	4
VDDRF_SW	Supply pin for the RF	VDDRF_SW		P/A		A9	47
VDDSYN_SW	Supply pin for the radio synthesizer			P/A		B8	45
VSSRF	RF analog ground		I/O	P		B9	46
XTAL48_N	Negative input for the 48 MHz xtal block		I/O	A		A6	43
XTAL48_P	Positive input for the 48 MHz xtal block		I/O	A		A8	44
VDDPA	Radio power amplifier voltage supply	VDDPA	I/O	P/A		C11	2
VSSPA	Radio power amplifier ground		I/O	P		D11	3
RF	RF signal input/output (Antenna)	RF	I/O	A		B11	1
VPP	Flash high voltage access	VPP	I/O	A		J6	17

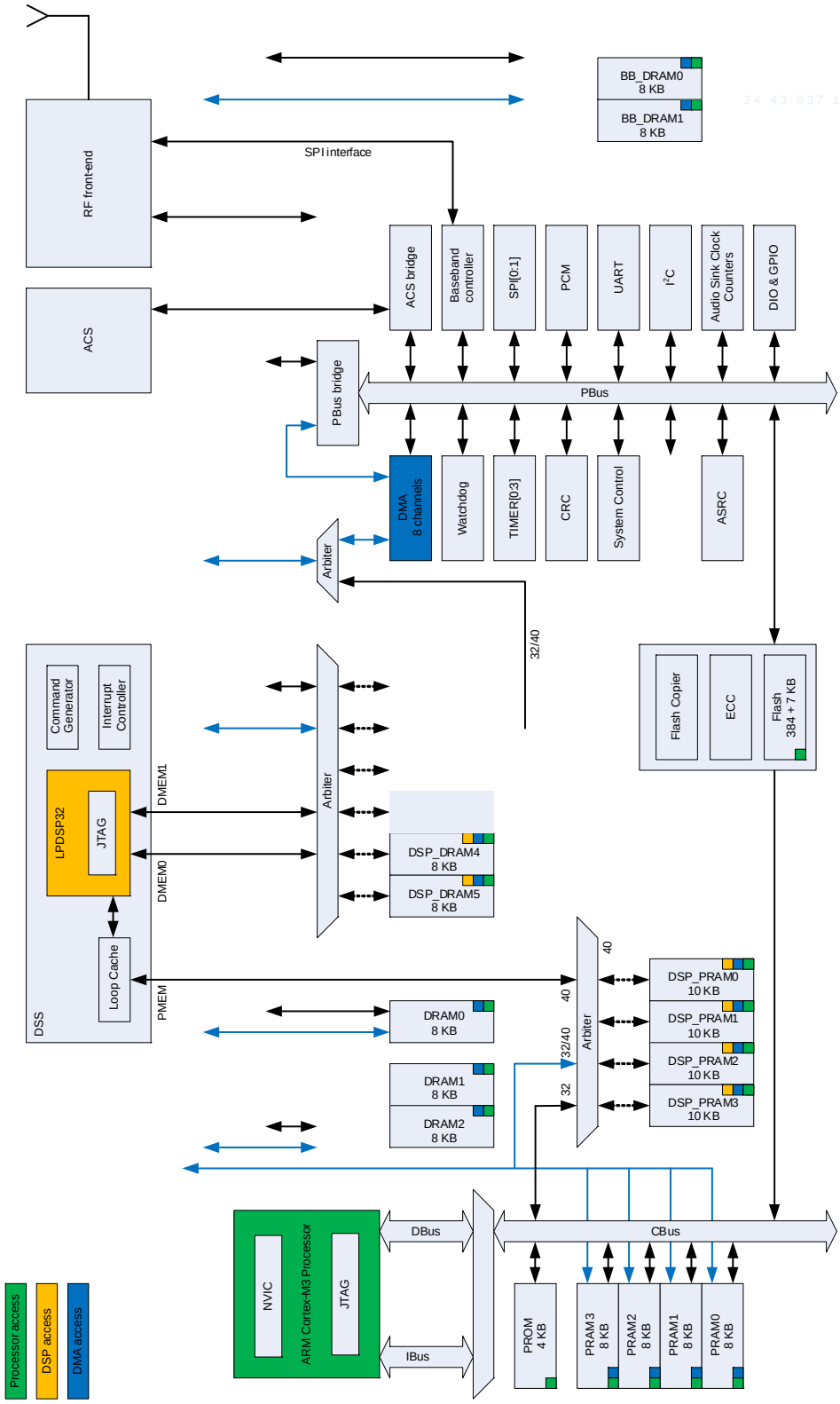

Figure 4. RSL10 Architecture

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Baseband Controller and Software Stack

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Arm Cortex−M3 Processor Subsystem

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Arm Cortex−M3 Processor

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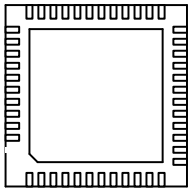
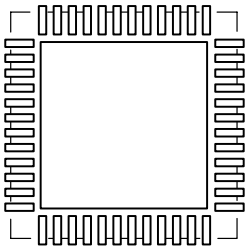
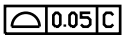
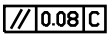
Table 10. RSL10 MEMORY STRUCTURES

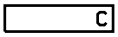
Memory Type	Data Width	Memory Size	Accessed by
Program memory (ROM)	32	4 kB	Arm Cortex−M3 processor
Program memory (RAM)	32		











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