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FEATURES

• Arm Cortex-M3 Processor: A 32-bit core for real-time applications, specifically developed to enable high-performance low-cost platforms for a broad range of low

RSL10 INTERNAL BLOCK DIAGRAM

The block diagram of the RSL10 chip is shown in Figure 1.

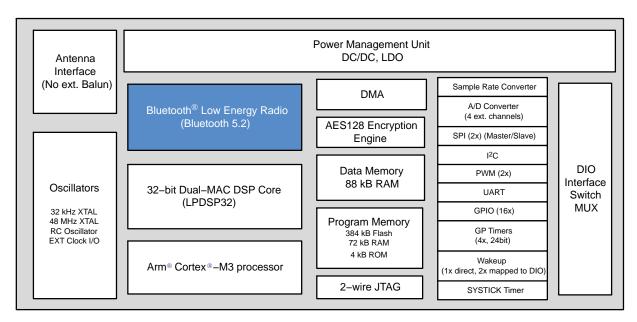




Table 1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VBAT	Power Suppl0Ryoltage		3.63	V
VDDO	I/O SuppI0Ryoltage (Note 1)		3.63	V



Table 2. RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Conditions	Min	Тур	Max	Unit
Supply Voltage Operating Range	VBAT	Input supply voltage on VBAT pin (Note 4)	1.18	1.25	3.3	V
Functional Temperature Range	T functional		-40	-	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. In order to be able to use a VBAT Min of 1.1 V, the following reduced operating conditions should be observed:

- Maximum Tx power 0 dBm.

- SYSCLK \leq 24 MHz.

Functional temperature range limited to 0–50°C

The following trimming parameters should be used:

- VCC = 1.10 V

– VDDC = 0.92 V

- VDDM = 1.05 V, will be limited by VCC at end of battery life

- VDDRF = 1.05 V, will be limited by VCC at end of battery life. VDDPA should be disabled

RSL10 should enter in end–of–battery–life operating mode if VCC falls below 1.03 V. VCC will remain above 1.03 V if VBAT ≥ 1.10 V under the restricted operating conditions described above.

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

Unless otherwise noted, the specifications mentioned in the table below are valid at 25° C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC-DC (buck) mode.

Description	otion Symbol Conditions		Min	Тур	Max	Unit
OVERALL						
Current consumption RX, V_{BAT} = 1.25 V, low latency	I _{VBAT}	RX Mode, onsemi proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay.		1.8		mA
Current consumption TX, V_{BAT} = 1.25 V, low latency	I _{VBAT}	TX Mode, onsemi proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay. Transmit power: 0 dBm		1.8		mA
Current consumption RX, V_{BAT} = 1.25 V	I _{VBAT}	RX Mode, onsemi proprietary audio streaming protocol at 7 kHz audio BW, 37 ms delay.		1.15		mA
Deep sleep current, example 1, V _{BAT} = 1.25 V	lds1	Wake up from wake up pin or DIO wake up.		50		nA
Deep sleep current, example 2, V _{BAT} = 1.25 V	lds2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.		90		nA
Deep sleep current, example 3, V _{BAT} = 1.25 V	lds3	As Ids2 but with 8 kB RAM data retention.		300		nA
Standby Mode current, V_{BAT} = 1.25 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.		30		μΑ
Current consumption RX, $V_{BAT} = 3 V$	I _{VBAT}	RX Mode, onsemi proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay.		0.9		mA
Current consumption TX, $V_{BAT} = 3 V$	I _{VBAT}	TX Mode, onsemi proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay. Transmit power: 0 dBm		0.9		mA
Deep sleep current, example 1, $V_{BAT} = 3 V$	lds1	Wake up from wake up pin or DIO wake up.		25		nA
Deep sleep current, example 2, $V_{BAT} = 3 V$	lds2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.		40		nA
Deep sleep current, example 3, $V_{BAT} = 3 V$	lds3	As Ids2 but with 8 kB RAM data retention.		100		nA
Standby Mode current, $V_{BAT} = 3 V$	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.		17		μΑ



Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued) Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC-DC (buck) mode.

Description	Symbol	Conditions	Min	Тур	Max	Unit
EEMBC ULPMark BENCHMARK,	CORE PROFILE	E				
ULPMark CP 3.0 V		Arm Cortex–M3 processor running from RAM, VBAT= 3.0 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1090		ULP Mark
ULPMark CP 2.1 V		Arm Cortex–M3 processor running from RAM, VBAT= 2.1 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1260		ULP Mark
EEMBC CoreMark BENCHMARK	for the Arm Cor	rtex-M3 Processor and the LPDSP32 DSF)			
Arm Cortex–M3 processor running from RAM		At 48 MHz SYSCLK. Using the IAR 8.10.1 C compiler, certified		159		Core Mark
LPDSP32 running from RAM		At 48 MHz SYSCLK Using the 2020.03 release of the Synopsys LPDSP32 C compiler		174		Core Mark
Arm Cortex–M3 processor and LPDSP32 running from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK		123		Core Mark/ mA
Arm Cortex–M3 processor and LPDSP32 running from RAM, VBAT = 3 V		At 48 MHz SYSCLK		293		Core Mark/ mA
Arm Cortex–M3 processor running CoreMark from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK (processor consumption only)		29.1		μA/MHz
Arm Cortex–M3 processor running CoreMark from RAM, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		12.3		μA/MHz
Arm Cortex–M3 processor running CoreMark from Flash, VBAT = 1.25 V		At 48 MHz SYSCLK (processor consumption only)		34.3		μA/MHz
Arm Cortex–M3 processor running CoreMark from Flash, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		14.6		μA/MHz
LPDSP32 running CoreMark from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK (processor consumption only)		19.5		μA/MHz
LPDSP32 running CoreMark from RAM, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		8.2		μA/MHz
INTERNALLY GENERATED VDDC	: Digital Block	Supply Voltage				
Supply voltage: operating range	VDDC		0.92	1 15	1.32	

	Supply voltage: operating range	VDDC	0.92	1.15	1.32
					(Note 5)
1		•		•	

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued) Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC–DC (buck) mode.

Description	Symbol	Conditions	Min	Тур	Max	Unit

INTERNALLY GENERATED VDDPA: Optional Radio Power Amplifier Supply Voltage





 Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)

 Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC-DC (buck) mode.

Description	Symbol	Conditions	Min	Тур	Max	Unit
ADC						
Resolution	ADC _{RES}		8	12	14	bits
Input voltage range	ADC _{RANGE}		0		2	V
INL	ADCINL		-2		+2	mV
DNL	ADC _{DNL}		–1		+1	mV
Channel sampling frequency	ADC _{CH_SF}	For the 8 channels sequentially, SLOWCLK = 1 MHz	0.0195		6.25	kHz
32 kHz ON-CHIP RC OSCILLAT	OR	• •				
Untrimmed Frequency	Freq _{UNTR}		20	32	50	kHz
Trimming steps	Steps			1.5		%
3 MHz ON-CHIP RC OSCILLATO	DR					
Untrimmed Frequency	Freq _{UNTR}		2	3	5	MHz
Trimming steps	Steps			1.5		%
Hi Speed mode	Fhi			10		MHz

32 kHz ON-CHIP CRYSTAL OSCILLATOR

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued) Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC–DC (buck) mode.

Description	Symbol	Conditions	Min	Тур	Max	Unit
FLASH SPECIFICATIONS						
Endurance for sections NVR1, NVR2, and NVR3 (6 kB in total)			1000			write/ erase cycles
Retention			25			years



Table 8. BUMP AND COATING SPECIFICATIONS

Subject	Specification				
Bump metallization	Sn 97.7%/Ag 2.3%				

Backside coating specification

Pad Name	Description	Power Domain	I/O	A/D	Pull	Pad #, WLCSP	Pad #, QFN48
VBAT	Battery input voltage	VBAT	Ι	Р		K5,K7,K10	9
VDC	DC–DC output voltage to external LC filter		0	А		J11	10
VCC	DC-DC filtered output		I	P/A		K11	12
XTAL32_IN	Xtal input pin for 32 kHz xtal		I/O	А		L10	14
XTAL32_OUT	Xtal output pin for 32 kHz xtal		I/O	А		L11	13
VSSA	Analog ground		I/O	Р		E10	8
RES	RESERVED		I	D	D	F8	11
VDDA	Charge pump output for analog and flash supplies	VDDA	I/O	P/A		F11	5
VDDRF	LDO's output for radio voltage supply		I/O	P/A		A11	48
CAP0	Pump capacitor connection		0	А		H11	7
CAP1	Pump capacitor connection		0	А		G10	6
AOUT	Analog test pin		0	А		L6	4
VDDRF_SW	Supply pin for the RF	VDDRF_SW		P/A		A9	47
VDDSYN_SW	Supply pin for the radio synthesizer			P/A		B8	45
VSSRF	RF analog ground		I/O	Р		B9	46
XTAL48_N	Negative input for the 48 MHz xtal block		I/O	А		A6	43
XTAL48_P	Positive input for the 48 MHz xtal block		I/O	А		A8	44
VDDPA	Radio power amplifier voltage supply	VDDPA	I/O	P/A		C11	2
VSSPA	Radio power amplifier ground]	I/O	Р		D11	3
RF	RF signal input/output (Antenna)	RF	I/O	А		B11	1
VPP	Flash high voltage access	VPP	I/O	А		J6	17

Table 9. CHIP INTERFACE SPECIFICATIONS



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ARCHITECTURE OVERVIEW

The architecture of the RSL10 chip is shown in Figure 4.

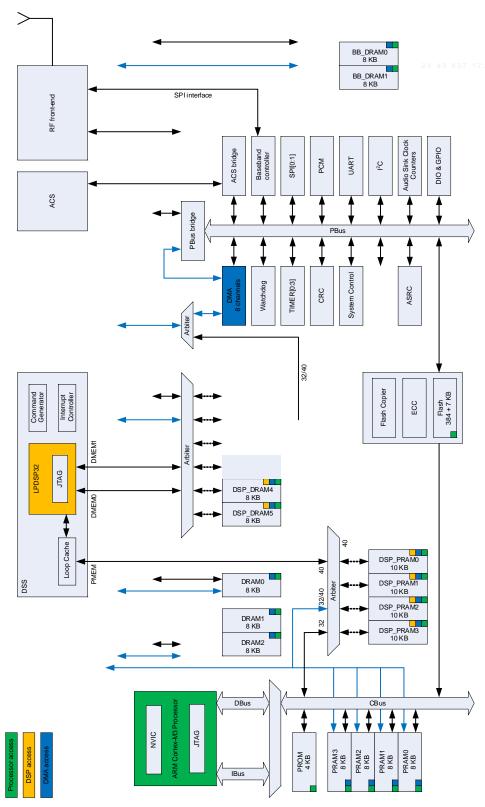


Figure 4. RSL10 Architecture

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The 2.4 GHz radio front-end contains a full transceiver with the following features:

- Manchester encoding
- Data whitening

The 2.4 GHz radio front–end contains also a highly–flexible digital baseband–in terms of modulations, configurability and programmability – in order to support Bluetooth Low Energy technology, DSSS, and proprietary protocols. It allows for programmable data rates from 62.5 kbps up to 2 Mbps, FSK with programmable pulse shape and modulation index.

The 2.4 GHz radio front-end also includes Manchester encoding and Data whitening. Its packet handling includes:

- Automatic preamble and sync word insertion
- Automatic packet length handler
- Basic address check
- Automatic CRC calculation and verification with a programmable CRC polynomial
- Multi-frame support
- 2x128 byte FIFOs

Baseband Controller and Software Stack

The RSL10 Bluetooth baseband controller is connected to the radio front-end. It configures the physical layer of the RSL10 for use as a Bluetooth Low Energy technology device. It provides access and support for the Direct-Test Mode (DTM) layer for RF testing, and it implements portions of the link layer and other controller level components from the Bluetooth stack. It is dedicated to low level bitwise operations and data packet processing.

Arm Cortex-M3 Processor Subsystem

The Arm Cortex–M3 processor subsystem includes the Arm Cortex–M3 processor, which is the master processor of the RSL10 chip. It also contains the Bluetooth baseband controller, and all interfaces and other peripherals.

Arm Cortex-M3 Processor

The Arm Cortex–M3 processor is a state–of–the–art 32–bit core with embedded multiplier and ALU for handling typical control functions. Software development is done in C.

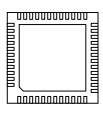
It features a low gate count, low interrupt latency, and low-cost debug functionality. It is primarily intended for deeply embedded applications that require low power

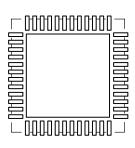


Table 10. RSL10 MEMORY STRUCTURES

Memory Type	Data Width	Memory Size	Accessed by
Program memory (ROM)	32	4 kB	Arm Cortex–M3 processor
Program memory (RAM)	32		







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