ORDERING INFORMATION

Device	Flash Memory	Package	Shipping
NCH-RSL15-284-101Q40-ACG	284 KB	QFN40	1500 Tape/Reel
NCH-RSL15-512-101Q40-ACG	512 KB	QFN40	1500 Tape/Reel
NCH-RSL15-512-101WC40-ABG	512 KB	WLCSP40	1500 Tape/Reel

APPLICATIONS

Connected Device

- Drug Injection Pens
- Blood Glucose Meters
- Wearable Bracelets
- Blood Analyzers
- Virus Detectors
- Smart Toothbrushes
- Heart Rate Monitors
- Bottle Caps
- Sleep Monitors
- Avalanche Detectors
- Electronic Pens
- Electronic Bikes
- Bicycle Computers
- Pet Trackers
- E−Stethoscopes
- Shavers
- Vacuum Cleaners
- SpO2 Monitors
- Wearable Head Bands

Smart Building

- Electronic Access Badges
- Air Filter Sensors
- Windows Surveillance
- Smoke Alarms
- Key Pads
- Energy Harvesting Switches
- HVAC Systems
- Vending Machines
- Lighting Control

Smart Industry

- Electronic Tags
- Power Tools
- Shopping Cart Trackers
- Coldchain Monitors
- Electronic Labels
- Beverage Dispensers
- Charge Control Systems
- Worker Safety Applications
- Battery Management Systems
- Machine Monitors
- Data Loggers
- Helmets
- Pellet Tracking
- Electronic Wheel Nuts
- Food Tracking Sensors

Smart Home

- Smart Circuit Breakers
- Smart Thermometers
- Smart Light Switches
- Smart Meters
- Coffee Makers
- Smart Refrigerators
- Air Purifiers
- Garage Door Controls
- Sprinkler Control Systems

Smart City

- People and Asset Tracking
- Door Access Control
- Fleet Management Systems
- Outdoor Robots
- Bioprocessing Equipment
- Educational Robots

HIGH−LEVEL BLOCK DIAGRAM

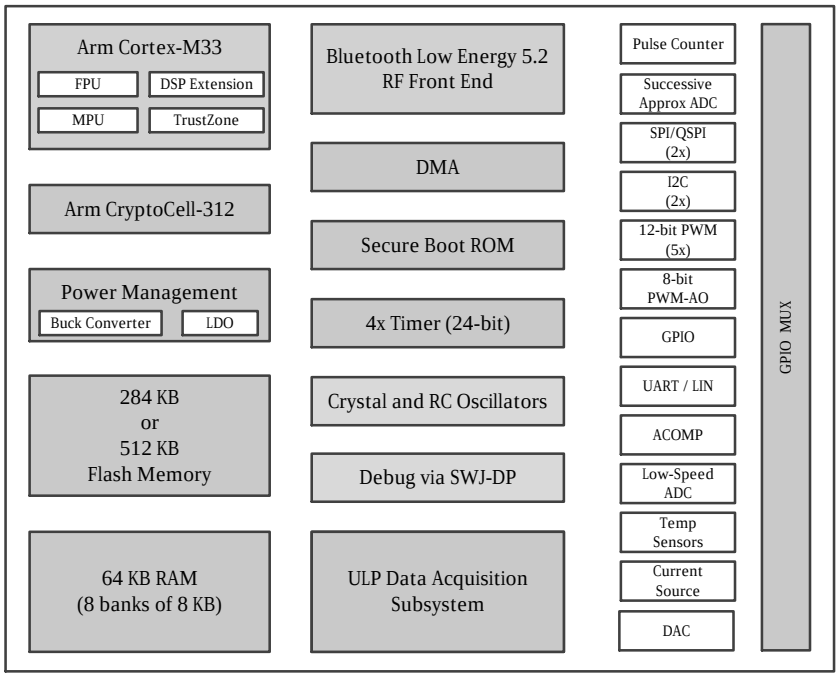


Figure 1. High−Level Block Diagram

FEATURES

Software Development Kit

Contains Eclipse−based **onsemi** IDE plus support for other industry standard development environments, Bluetooth protocol stack, sample applications, libraries and many other software components and tools to enable rapid

Cybersecurity Platform

The Cortex−M33 processor with TrustZone Armv8−M security extensions forms the basis of the security platform that is extended with Arm CryptoCell−312.

Secure Boot with Root of Trust

The secure boot ROM authenticates firmware in flash with a certificate−based mechanism using a private−public key scheme. This is the basis of the hardware Root of Trust. This same mechanism ensures continuity of the hardware Root of Trust after secure Firmware−Over−The−Air (FOTA) update.

Data and Application Encryption

User available cryptographic services including AES−128, AES−256, SHA−256, Hash Message Authentication Code (HMAC), PKA (Public Key Accelerator), ChaCha and AIS−31 compliant True Random Number Generator (TRNG) allow for development of custom proprietary security solutions.

TrustZone

Enables secure software access control to protect critical software and hardware resources.

Secure Lifecycle State Management

Lifecycle states refers to the multiple states RSL15 could go through during its lifetime. The first lifecycle state is the Chip Manufacture (CM) Lifecycle State. The device manufacture transitions to the Device Manufacture (DM) Lifecycle State. At field deployment, it is transitioned to the Secure (SE) Lifecycle State. A Return to Manufacturer (RMA) State is also available. Lifecycle state management ensures the authenticity, integrity and confidentiality of code and data belonging to different stakeholders at each lifecycle.

In addition to the Secure Lifecycle States, an Energy Harvesting (EH) Mode is available for applications that require fast cold startup (initial application of VBAT) but do not require secure boot with Root of Trust. This mode is especially useful when RSL15 is used in energy harvesting systems.

RF Subsystem

The RSL15 2.4 GHz radio front−end implements the physical layer for the Bluetooth Low Energy standard and other standard, proprietary, or custom protocols.

It operates in the worldwide deployable 2.4 GHz ISM band (2.4000 to 2.4835 GHz).

RF Architecture

The 2.4 GHz radio front−end is based on a low−IF architecture and comprises the following building blocks:

- High performance single−ended RF port which alleviates the need for an external balun
- On−chip matching network with 50 Ω RF input
- Low power LNA (low noise amplifier), and mixer
- PA (Power Amplifier) with up to +6 dBm output power for Bluetooth
- RSSI (Received Signal Strength Indication) with 60 dB nominal range with 1 dB steps (not considering AGC)
- Fully integrated ultra−low power frequency synthesis with fast settling time, with direct digital modulation in transmission (pulse shape programmable)
- 48 MHz XTAL reference
- Fully−integrated FSK−based modem with programmable pulse shape, data rate, and modulation index
- Digital baseband (DBB) with link layer functionalities, including automatic packet handling with preamble & sync, CRC, and separate Rx and Tx 128−bytes FIFOs
- The 2.4 GHz radio front−end contains also a highly−flexible digital baseband – in terms of modulation schemes, configurability and programmability – in order to support Bluetooth Low Energy technology and proprietary protocols. It allows for programmable data rates from 62.5 kbps up to 2 Mbps, FSK with programmable pulse shape and modulation index.
- The 2.4 GHz radio front−end also includes Manchester encoding and Data whitening. The packet handling includes:
  - Automatic preamble and sync word insertion
  - Automatic packet length handler
  - Basic address check
  - Automatic CRC calculation and verification with a programmable CRC polynomial
  - Multi−frame support
- Coexistence signals to identify the RF front−end is busy for Bluetooth or other traffic

Bluetooth Low Energy

RSL15 is Bluetooth 5.2 certified with the following Bluetooth LE features:

- Angle of Arrival (AoA) and Angle of Departure (AoD)
- LE Long Range (Coded PHY)
- 2 Mbit PHY (High Speed)
- LE Extended Advertising
- High Duty Cycle Non−Connectable Advertising
- LE Channel Selection Algorithm #2
- Advertising Channel Index
- GATT Caching
- HCI support for debug keys in LE Secure Connections
- Sleep clock accuracy update mechanism
- ADI field in scan response data
- Host channel classification for secondary advertising
- Periodic Advertising Sync Transfer
- Backwards compatibility and support for earlier Bluetooth Low Energy specifications including 5.1, 5.0, 4.2, 4.1 and 4.0

Power Management

The flexible power management of RSL15 allows for a wide range of battery voltages without the need for external power conversion. Two key modes of the DC−DC converter are:

1. BUCK Mode Operation
2. LDO Mode Operation

The power management unit is shown in Figure 3.

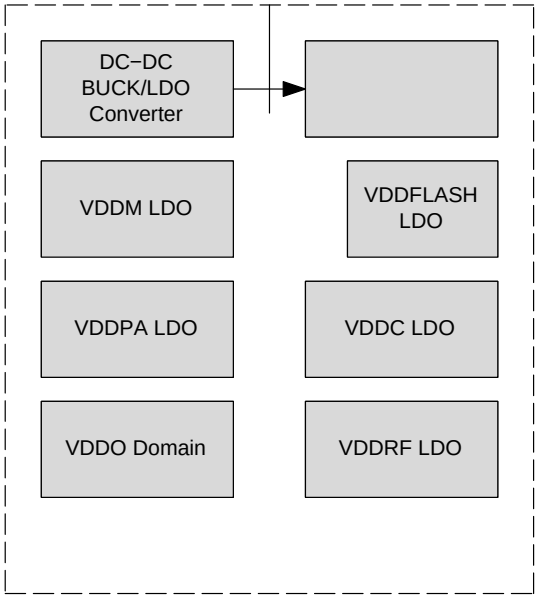


Figure 3. Power Management Unit

Peripherals and Subsystems Availability in Power Modes

The different power modes allow for low power operation in many types of applications. When applications utilize one or more external sensors that require continued biasing regardless of the power mode of RSL15, it may be possible to use the VDDA voltage for this purpose.

VDDA can be kept active even in Sleep, Smart Sense and Standby Modes.

Table 2 describes the peripherals available in all power modes.

Table 2. POWER MODE PERIPHERAL AVAILABILITY

Component	Power Mode				
	Run	**Idle**	**Standby**	**Smart Sense**	**Sleep**
Processor	On	On	Off	Off	Off
Baseband/RF	On	Off	Off	Off	Off
RAM Retention	n/a	n/a	Available	Available	Available
CryptoCell	On	On	On or Off	On or Off	On or Off
RTC	On	On	On or Off	On or Off	On or Off
ULP Data Acquisition Subsystem	On	On	On or Off	On or Off	Off
Successive Approximation ADC	On	On	On or Off	On or Off	Off
Pulse Counter	On	On	On or Off	On or Off	Off
Comparator	On	On	On or Off	On or Off	On or Off
DAC	On	On	Off	Off	Off
ACS−PWM	On	On	On or Off	On or Off	On or Off
PWM	On	On	Off	Off	Off
Low Speed ADC	On	On	Off		

The ULP Data Acquisition Subsystem has various features to further reduce power consumption such as Burst Sampling Mode, which allows for bursts of high speed sampling followed by an adjustable delay between sampling bursts.

The pulse counter can be configured to accept inputs from any of GPIO[3:0]. It counts pulses from these GPIOs during a set window ranging from 1 to 1024 clock cycles (based on a 32 kHz clock).

Overall, the ULP Data Acquisition Subsystem operation can be summarized as follows:

Accumulation

- An accumulation can be done with a configured number of samples ranging from 1 to 16 samples
- This mode is enabled when SUM_EN is set on Figure 4
- The accumulated value is stored in the FIFO

Threshold Detection

- Two thresholds can be configured: one when the input value goes higher than the threshold, and one when the input value goes lower than the threshold
- This mode allows the system to wake up after a configured number of consecutive samples generated are greater than or lower than the configurable threshold.

Acquisition

- Acquired samples are stored in the FIFO. FIFO size can be 1 to 16 samples

Clocking

Oscillators

The following oscillators are available:

- 48 MHz crystal oscillator (RFCLK) typically used in RUN Mode when RF operation is required. Prescalers exist to provide divided clocks (including system clock) to other parts of the system
- A fast RC oscillator (RCCLK) can provide an alternative to the 48 MHz crystal oscillator. However, RF operation is not possible using the fast RC Oscillator
- A 32 kHz crystal oscillator (XTAL32K) typically used in Sleep and Standby Modes for precision timing and to maintain the real−time clock (RTC)
- A slow RC oscillator (RC32) that can be an alternative to the 32 kHz crystal oscillator for certain use cases.

Clock Management

Flexible clock management allows the different clock sources to be used in power−efficient ways and to minimize external components. Internal RC oscillators can be used for fast startup and then easily switched to crystal oscillators when precision timing is required. Additionally, clocks can be sourced externally with the 48 MHz and 32 kHz clock inputs.

A built−in clock detector ensures a proper system reset in case the system clock goes below 2 kHz.

General Purpose Input/Output (GPIO)

RSL15 contains highly flexible general purpose input/output (GPIO) pins that can be configured as digital input or output, communication interfaces, clocks, wakeup sources or analog functions. Communication interfaces can be routed to any GPIO. Other functions are available on select GPIO, see section Pin Definition and Multiplexing.

Each GPIO has a software configurable pull up/down resistor, debounce LPF for I2C and four drive strengths options.

Analog

Successive Approximation ADC (SAR ADC)

The Successive Approximation ADC (SAR ADC) generates 12−bit samples up to 2 Msps sample frequency.

The SAR ADC is auto calibrated during operation for optimal INL/DNL performance.

Low Speed ADC Converter (LSAD)

This is a combined integrating and algorithmic ADC that has a resolution varying from 8 to 14 bits depending on configuration. While converting, the input signal can be integrated across one or more clock cycles (depending on configuration). ADC sampling rate can be up to 50 ksps. This ADC converter is also used to monitor the VBAT input voltage. It can also be configured to measure single ended or differential input voltages.

Pulse Counter

A pulse counter can be driven by one of GPIO[3:0]. It counts pulses from these GPIOs during a set interval.

Analog Comparator

RSL15 contains a low−power comparator that can be active in Standby, Sleep and Smart Sense mode. It has 3 different settings to trade off response time with power consumption, Low Power, Normal and High Speed, see section Analog Comparator Specifications (ACOMP).

DAC

RSL15 contains a low−power DAC that can be used for sensor biasing purposes. To optimize power consumption there is also a buffer that can be disabled if the load is high impedance.

Current Source

A built−in current source with adjustable output from 1 μA to 16 μA. The current source may be applied for temperature measurements using an external thermistor connected to a GPIO.

Memory Map

The RSL15 memory map is shown in Figure 5 (512 KB flash version only).

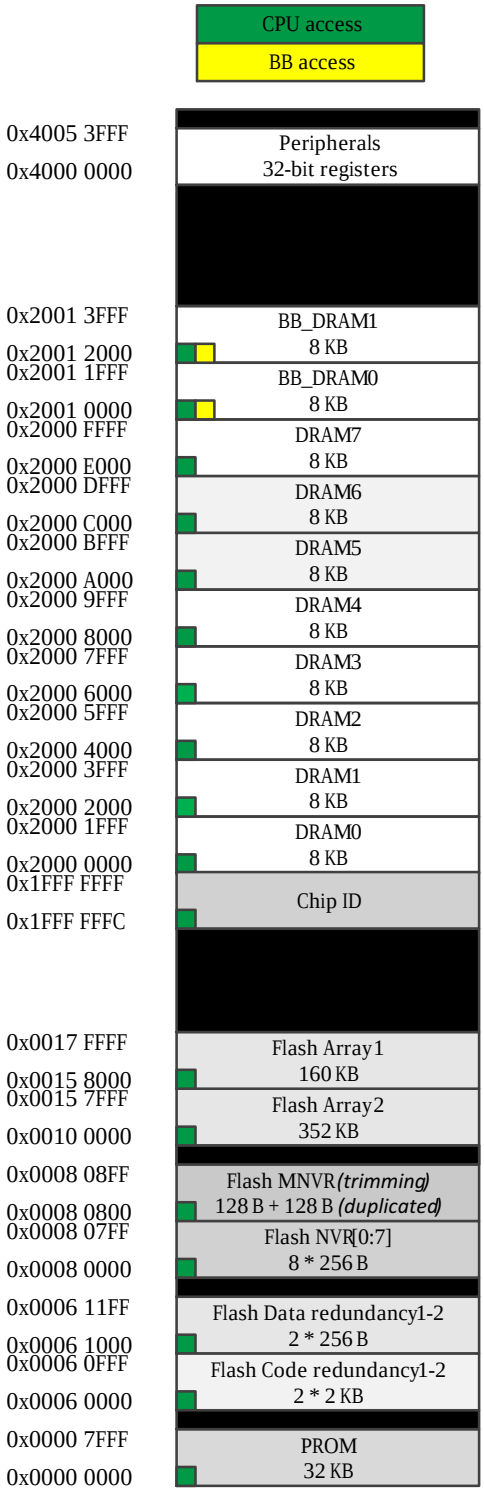


Figure 5. RSL15 Memory Map

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VBAT	Power supply voltage input		3.63	V
VDDO	Digital I/O supply voltage input		3.63	V
VSSRF	RF front−end ground	−0.3		V
VSSA	Analog ground	−0.3		V
VSSC	Digital ground	−0.3		V
Vin	Voltage at any input pin	VSSC−0.3	VDDO + 0.3	V
Vin to LSAD	Voltage at GPIO selected as LSAD input	VSSA − 0.3	VDDA + 0.3	V
RF	Maximum RF Input Power		18	dBm
T storage	Storage temperature range (Note 1)	−40	125	°C

Stresses exceeding those listed in the Absolute Maximum Ratings table may damage the device.

CAUTION: Class 2 ESD Sensitivity, JESD22 – A114 – B HBM +/−2000 V on all pins
CDM ESD Compliance on all pins: ±500 V
Latch−up protection of ±100mA, EIA/JESD78E on all pins

1. Storage temperature applies after soldering to PCB.

General Operating Conditions

Table 4. GENERAL OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC−DC Converter Input Voltage	VBAT	BUCK Mode	1.4		3.6	V
		LDO Mode	1.2		3.6	
VBAT supply rise time		Maximum rate of voltage rise			0.1	V/μs
DC−DC Converter / LDO Output Voltage (Note 2)	VCC		1	1.2	1.32	V
Analog blocks supply voltage output (Note 2)	VDDA	VDDA is generated by a charge pump that doubles the VCC voltage				

Power Consumption

RF Current Consumption

Table 5 shows key peak current consumption values for RF activity. Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C, VBAT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT ≤ 1.4 V), 48 MHz (RFCLK) active, Radio ON and internal supplies trimmed to factory defaults.

Table 5. RF CURRENT CONSUMPTION

Operating Conditions	VBAT	DC Conversion	Min	Typ	Max	Unit
Radio Receive Mode Rx @ 125 kbps, 2.4 GHz 8 MHz system clock						

Run Mode Current Consumption

Table 6 shows key current consumption values for Run Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C, VBAT = VDDO (Buck

Standby Mode Current Consumption

Table 8 shows key current consumption values for Standby Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C, VBAT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT ≤ 1.4 V), 48 MHz (RFCLK) inactive, Radio OFF and internal power supplies trimmed to factory defaults.

Table 8. STANDBY MODE CURRENT CONSUMPTION

Operating Conditions	Wakeup Source	VBAT	DC Conversion	Min	Typ	Max	Unit
Clocks stopped All peripherals disabled **8 KB RAM retained** 32 kHz RC32 inactive 32 kHz XTAL32K inactive	GPIO	3.0 V	BUCK Mode		17		µA
		1.8 V	BUCK Mode		20		
		1.25 V	LDO Mode		26		
Clocks stopped All peripherals disabled **16 KB RAM retained** 32 kHz RC32 inactive 32 kHz XTAL32K inactive	GPIO	3.0 V	BUCK Mode		17.5		µA
		1.8 V	BUCK Mode				

Sleep Mode Current Consump

Table 9 shows key current [redacted]n values for Sleep Mode. Unless otherwise noted[redacted]ications mentioned in the table below are valid at [redacted]AT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode fo[redacted].4 V), 48 MHz (RFCLK) inactive, Radio [redacted]nternal supplies trimmed to factory defaults.

Table 9. SLEEP MODE CURRENT CONSUMPTION

Operating Conditions	Symbol	Wakeup Source	VBAT	DC Conversion	Min	Typ	Max	Unit
Clocks stopped All peripherals disabled **No RAM retained** 32 kHz RC32 inactive 32 kHz XTAL32K inactive	Ids1	GPIO	3.0 V	BUCK Mode		36		nA
			1.8 V	BUCK Mode	3o 47K Mode			

ULP Data Acquisition Subsystem Performance

Table 10 shows key current consumption values for ULP Data Acquisition Subsystem in Smart Sense Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C, VBAT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT ≤ 1.4 V), 48 MHz (RFCLK) inactive, Radio OFF and internal supplies trimmed to factory defaults.

Table 10. ULP DATA ACQUISITION SUBSYSTEM PERFORMANCE

Operating Condition	Min	Typ	Max	Unit
Continuous ADC operation in Smart Sense mode with wakeup on ADC threshold Configuration/conditions: VBAT = 3 V, BUCK Mode, Successive Approximation ADC enabled and selected, XTAL32K, VREF = VBAT reference selected, ADC Fs = 256 sps, accumulation 4 samples. Processor would wake to Run mode by ADC threshold but this is not included in this measurement		206		nA
Continuous ADC operation in Smart Sense mode, wakeup on FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 KB RAM retained, XTAL32K, Successive Approximation ADC enabled, VREF = VBAT, ADC Fs = 1 ksps, accumulation 16 samples, FIFO Size 16. Processor wakes to Run mode every 256 ms to transfer samples to RAM		2.1		μA
Continuous ADC operation in Smart Sense mode, wakeup on FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 KB RAM retained. XTAL32K, Successive Approximation ADC enabled, VREF = VDDA, ADC Fs = 1 ksps, Accumulation 16 samples, FIFO Size 16. Processor wakes to Run mode every 256 ms to transfer samples to RAM		4.1		μA
Continuous Pulse Counter accumulation in Smart Sense mode, wakeup when FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 KB RAM retained, XTAL32K, Pulse Counter enabled, Pulse Count Interval 1000 ms, accumulation of 5 samples, result stored in FIFO. Processor wakes to Run mode every 5 s to transfer sample to RAM		348		nA

NOTE: Current values include increases due to workarounds imposed by errata in section ‘RSL15 Errata for Chip Identification 2.02.00’.

Table 12. EEMBC BENCHMARK SCORES

Table 15. 32 kHz CRYSTAL OSCILLATOR (XTAL32K) (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating current						

Successive Approximation ADC (SAR ADC) Specifications

Table 21. SUCCESSIVE APPROXIMATION ADC (SAR ADC) SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ADC reference voltage	VREF	VBAT selected as reference VREF	1.8		3.6	V
		GPIO[9] selected as reference VREF	1.8		VDDO	V
Resolution				12		Bits
Input voltage range			0		VREF	V
Differential input voltage range			−VREF		VREF	V
Sampling rate		VREF ≥ 2.5 V			2	Msps
		VREF 2.0 V to 2.5 V			0.5	Msps
		VREF 1.8 V to 2.0 V			0.125	Msps
LSB weight		12 bits resolution at VREF = VBAT = 3.6 V		1.6		mV
Absolute gain error			−2		+2	%
INL			−4		4	LSB
DNL			−1.5		1.5	LSB
Offset		After calibration	−5		5	LSB
Gain error		After calibration	−1		1	%
Noise		RMS noise in LSB for a constant input voltage			2	LSBrms
Input capacitance				1		pF
Array calibration time				650		cycles
Current consumption				26		µA / Msps

Low Speed ADC Converter (LSAD) Specifications

Table 22. LOW SPEED ADC CONVERTER (LSAD) SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution	ADC_{RES}		8	12	14	bits
Input voltage range	ADCRANGE		0		2	V
INL	ADC_{INL}		−2		+2	mV
DNL	ADC_{DNL}		−1		+1	mV
Channel sampling frequency	ADCCH_SF	8 channels are converted sequentially, ADC running at 50 kHz	0.0195		6.25	kHz

Table 23. DAC SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max

4095 329.4422.7371 Tm(

Temperature Sensor Specifications

Table 24. TEMPERATURE SENSOR SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Accuracy potential		Requires calibration by the customer	−2		2	°C
Temperature sensor output voltage @ 25°C		Uncalibrated	0.9	0.95	1	V
Temperature sensor gain @ 25°C				21.3		LSB/°C
Startup time		From enable to specified accuracy		100	200	µs
Active current consumption					10	µA

Pulse Counter Specifications

Table 25. PULSE COUNTER SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pulse width						µs
Pulse count duration		Using accumulation to reach max	0.976		16000	ms

RSL15 ERRATA FOR CHIP IDENTIFICATION 2.02.00

The chip identification can be derived by reading the Chip Version, Chip Major Revision and Chip Minor Revision bit fields.

The RSL15 Firmware Package version 1.5 contains implementations of the following errata workarounds. Table 9 and Table 10 in datasheet Rev. 4 include current increases due to workarounds imposed by these errata.

Some Registers Might Not Initialize Properly When Waking from Deep Sleep

When RSL15 wakes from deep sleep mode, some registers in the ACS might not be iJ/TT29l,sTw[pn27v

TYPICAL CONNECTION DIAGRAMS

It is recommend to have external access to a UART for general diagnostics and for wired communication during Bluetooth certification. It is also recommend to have a method to load new firmware during Bluetooth certification. Firmware can be loaded by any method such as the Serial Wire Debug (SWD) with pins SWDIO, SWCLK, VDDO (IO voltage domain) and a ground connection. Two GPIO must be externally accessible for the UART. The UART GPIO do not need to be permanently dedicated to UART in the final product as temporary provisions can be made to

LDO Mode Operation

Figure 7 shows RSL15 external components and connections for LDO Mode operation with GPIO Levels at GND and VBAT.

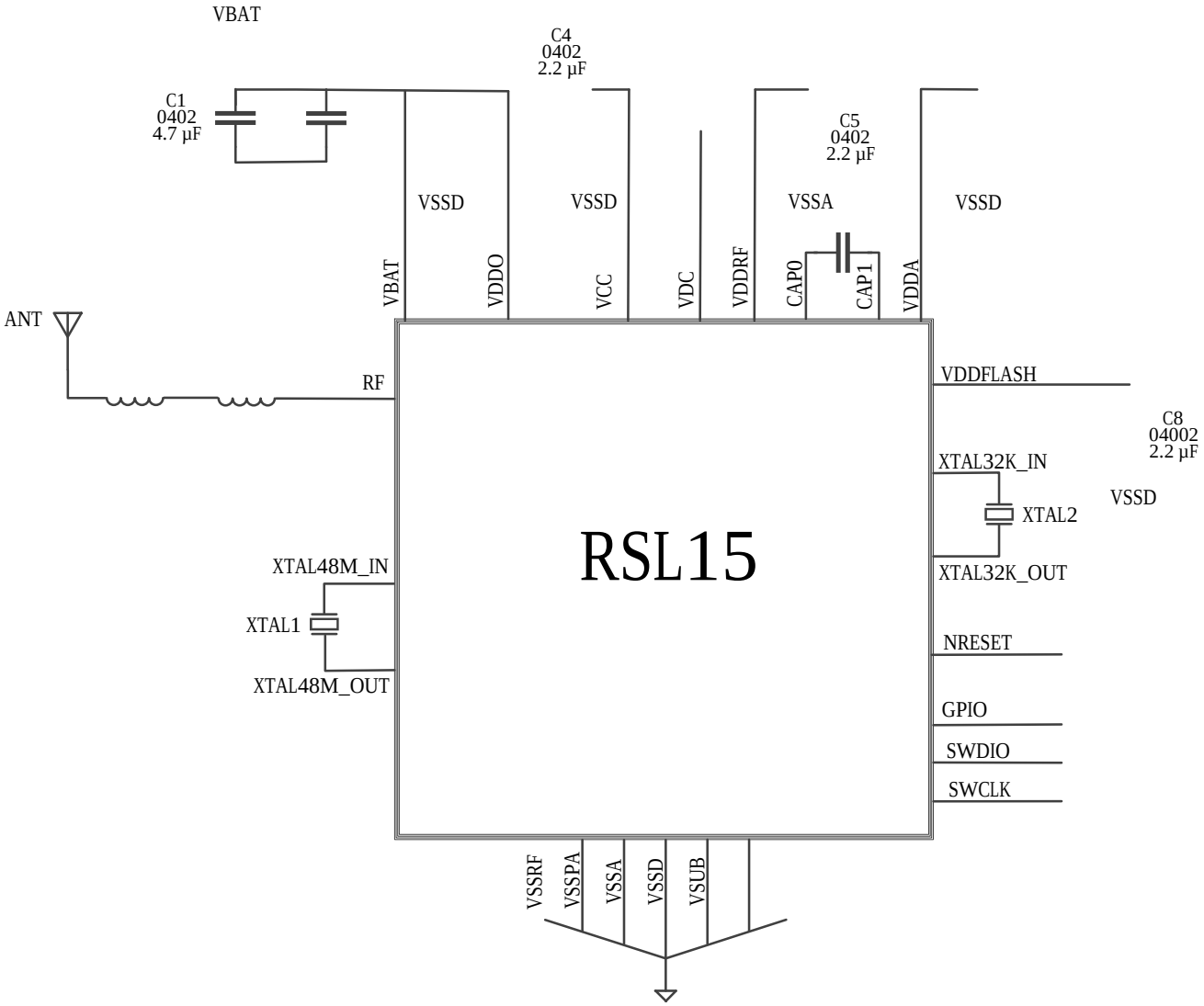


Figure 7. RSL15 LDO Mode Connection Diagram, VDDO = VBAT

External Component Overview

Table 27. RECOMMENDED EXTERNAL COMPONENTS

Components	Function	Recommended Typical Value	Nominal Tolerance
C1, C2	VBAT decoupling	4.7 μF // 100 pF (Note 9)	±20%
C3	VDDO decoupling	1 μF	±20%
C4	VCC decoupling	2.2 μF − GRM155C80J225KE95D, Murata − AMK105BJ225, Taiyo Yuden	±20%
C5	VDDRF decoupling	2.2 μF	±20%
C6	Pump capacitor for the charge pump	1 μF	±20%
C7	VDDA decoupling	1 μF	±20%
C8	VDDFLASH decoupling	2.2 μF	±20%
L1			

PIN DEFINITIONS

QFN40 Pin Out

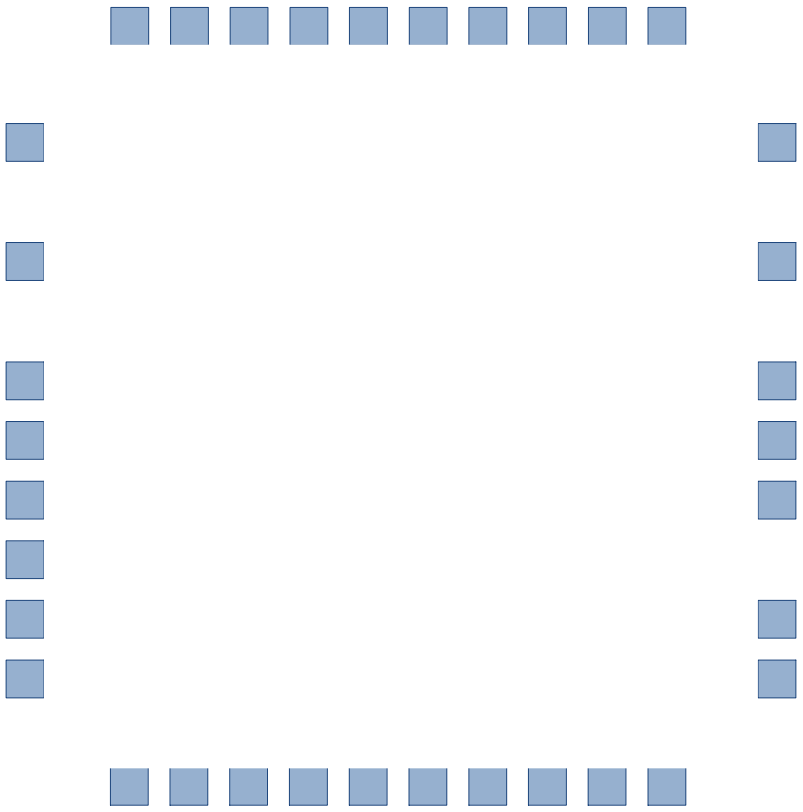


Figure 8. QFN40 Pin Out

RSL15

Pin Definition and Multiplexing

RSL15 has very flexible pad multiplexing capabilities. Most functions are available on any GPIO. Table 29: Pin Definition lists all pins and their functionality while Table 30: GPIO Multiplexing shows all multiplexed functions available on the GPIO.

Legend:
I = input; O = output; P = power;
Pull: PU = pull up; PD = pull down;

Table 29. PIN DEFINITION AND MULTIPLEXING

Pad Name	Description	Power Domain	Type	Pull	Pad #, QFN	Ball #, WLCSP
XTAL32K_IN	Input pin for 32 kHz XTAL	VBAT			1	E2
XTAL32K_OUT	Output pin for 32 kHz XTAL	VBAT			2	E1
NRESET	Reset pin	VDDO	I	PU	3	D1
VPP	Flash high voltage access, do not connect (NC)		P		4	D2
VSSD	Core logic ground		P		5	D3

Table 29. PIN DEFINITION AND MULTIPLEXING

Pad Name	Ball #,

Table 30. GPIO MULTIPLEXING

GPIO	Mode	Description
0:15	SLOWCLK (output) SYSCLK (output) USRCLK (output) RCCLK (output) SWCLK (output) EXTCLK (output) STANDBYCLK (output) SENSORCLK (output)	Clocking
0:15	UART0_RX UART0_TX / LIN0_TX LIN_RX SPI0_MOSI/DATA0 SPI0_MISO/DATA1 SPI0_DATA2 SPI0_DATA3 SPI0_CS SPI0_CLK SPI1_MOSI/DATA0 SPI1_MISO/DATA1 SPI1_DATA2 SPI1_DATA3 SPI1_CS SPI1_CLK I2C0_SCL I2C0_SDA I2C1_SCL I2C2_SDA PWM0 PWM1 PWM2 PWM3 PWM4 PWM0_INV PWM1_INV PWM2_INV PWM3_INV PWM4_INV PCM_SERI PCM_SER0 PCM_FRAME PCM_CLK	Interfaces

11. ACS−PWM has an equivalent 500 Ohm series resistor at the output.
12. RTC_CLK_OUTPUT output level is at VCC in Sleep Mode.

PCB LAYOUT GUIDELINES

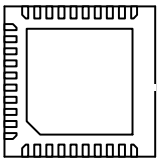
1. Decoupling capacitors should be placed as close to the related balls as possible
2. Differential output signals should be routed as symmetrically as possible
3. Analog input signals should be shielded as well as possible
4. Pay close attention to the parasitic coupling capacitors

5. Special care should be made for PCB design in order to obtain good RF performance
6. Multi−layer PCB should be used with a keep−out area on the inner layers directly below the antenna matching circuitry in order to reduce the stray capacitances that influence RF performance
7. All the supply voltages should be decoupled as close as possible to their respective pin with high performance RF capacitors. These supplies should be routed separately from each other and if possible on different layers with short lines on the PCB from the chip's pin to the supply source
8. Digital signals should not be routed close to the crystal or the power supply lines
9. Proper DC−DC component placement and layout is critical to RX sensitivity performance in DC−DC mode. Minimize parasitic capacitance and inductance on the VDC node as much as possible.
10. [QFN only]: Ground EP by vias to a ground plane and/or through at least two VSS pins to PCB surface ground.
11. [QFN only]: Connect SHLD pin to EP, and connect SHLD to an external ground trace shielding XTAL48M_IN from SWCLK.
12. [WLCSP only] On−chip RF inductor coils need a keep−out area on the top layer metal (refer to the keep−out zone in the WLCSP40 PACKAGE DIMENSIONS drawing)
13. [WLCSP only] Ground plain should be removed under XTAL +/− signal pins and lines to ensure parasitic capacitance is less than 1 pF

PACKAGE MARKING INFORMATION

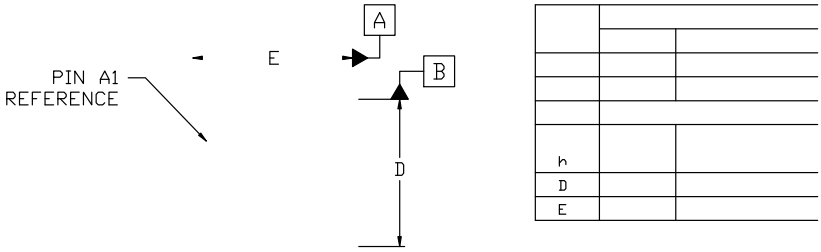
Chip Identification

System identification is used to identify different system components. For the RSL15 chip, the key identifier components and values are as follows:



WLCSP40 2.301x2.499x0.369
CASE 567HU
ISSUE O

DATE 29 APR 2022



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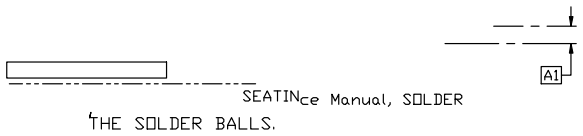

RECOMMENDED
MOUNTING FOOTPRINT