A571

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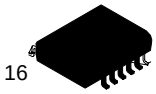
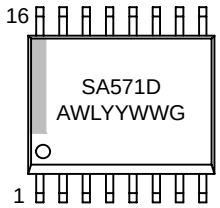
The SA571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full−wave rectifier to detect the average value of the signal, a linerarized temperature−compensated variable gain cell, and an operational amplifier.

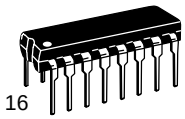
The SA571 is well suited for use in cellular radio and radio communications systems, mD, and N Packages*

MARKING DIAGRAMS

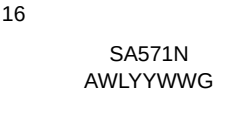


SOIC−16 WB
D SUFFIX
CASE 751G

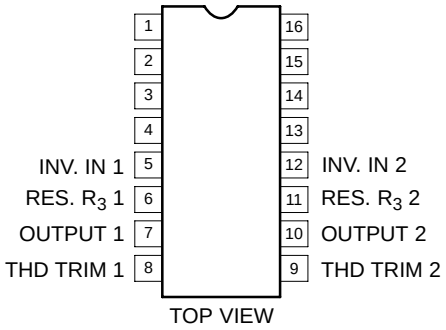




PDIP−16
N SUFFIX
CASE 648



PIN CONNECTIONS



*SOL − Released in Large SO Package Only.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

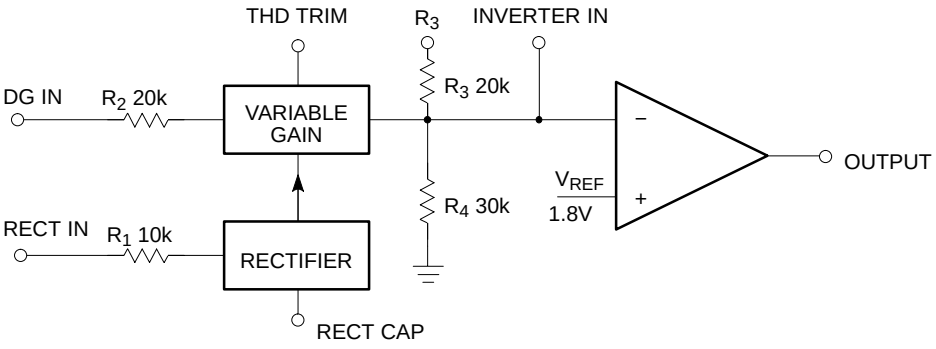


Figure 1. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Operating Voltage	V_{CC}	18	VDC
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature	T_J	150	°C
Power Dissipation	P_D	400	mW
Thermal Resistance, Junction−to−Ambient N Package D Package	R_{JA}	 75 105	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	−	6.0	−	18	V
Supply Current	I_{CC}	No Signal	−	4.2	4.8	mA
Output Current Capability	I_{OUT}	−	± 20	−	−	mA

Circuit Description

The SA571 compandor building blocks, as shown in the block diagram, are a full−wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full−wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively−coupled voltage inputs as shown in the following equation. Note that for capacitively−coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1 A.

$$G \propto \frac{|V_{IN} - V_{REF}|\,avg}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\,avg}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade−off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\, e^{\frac{-t}{\tau}} + G_{final}$$

$$\tau = 10k \times C_{RECT}$$

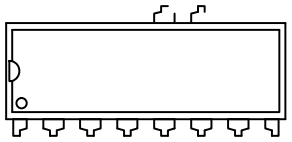
The variable gain cell is a current−in, current−out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively−coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

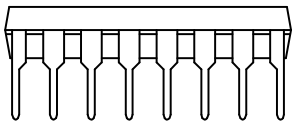
$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset

Figure 6 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6.0 dB, the gain control current will drop by a factor of 2, and so the gain will drop 6.0 dB. The output level at V_{OUT} will thus drop 12 dB, giving us the desired 2−to−1 expansion.

Figure 9





SOIC

−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.