STK672-732AN-E

Stepper Motor Driver IPM (Intelligent Power Module) Unipolar 2-Phase

ON Semiconductor®

www.onsemi.com

Overview

The STK672-732AN-E is a IPM for use as a unipolar, 2-phase stepper motor driver with PWM current control.

Applications

Office photocopiers, printers, etc.

Features

Built-in overcurrent detection function, overheat detection function (output current OFF).

Built-in power on reset function.
Phase signal input driver activated with an active Low and incorpororates a simulataneous ON prevention function.

ORDERING INFORMATION

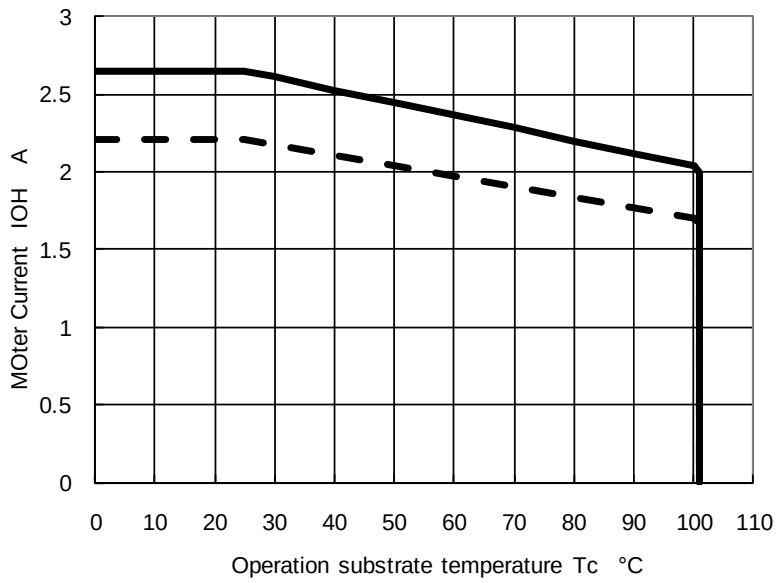
See detailed ordering and shipping information on page 26 of this data sheet.

October 2016 - Rev. 1

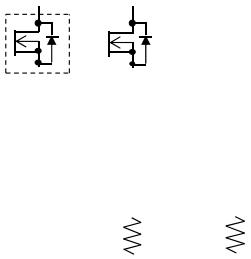
Publication Order Number :
STK672-732AN-E/D

Allowable Operating Ranges at Tc = 25 C

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage 1	V_{CC}	With signals applied	0 to 42	V
Operating supply voltage 2	V_{DD}	With signals applied	5 5%	V
Input high voltage	V_{IH}	Pins 10, 12, 13, 14, 15, 17, V_{DD} = 5 5%	2.5 to V_{DD}	V


3
2.5
2
1.5
1
0.5
0
MOter Current IOH A
0 10 20 30 40 50 60 70 80 90 100 110
Operation substrate temperature Tc °C

Block Diagram



Sample Application Circuit

Precautions

[GND wiring]

To reduce noise on the 5 V / 24 V system, be sure to place the GND of C01 in the circuit given above as close as possible to Pin 2 and Pin 6 of the IPM.

In addition, in order to set the current accurately, the GND side of RO2 of Vref must be connected to the shared ground terminal used by the Pin 18 (S.G) GND, P.G1 and P.G2.

[Input pins]

If V_{DD} is being applied, use care that each input pin does not apply a negative voltage less than 0.3 V to S. GND, Pin 18. Measures must also be taken so that a voltage equal to or greater than V_{DD} is not input.

Do not wire by connecting the circuit pattern on the P.C.B side to Pins 4, 8, or 11 on the N.C. shown in the internal block diagram.

Apply 2.5 V high level input to pins 10, 12, 13, 14, 15, and 17.

Since the input pins do not have built-in pull-up resistors, when the open-collector type pins 10, 12, 13, 14, 15, and 17 are used as inputs, a 1 to 20 k pull-up resistor (to V_{DD}) must be used.

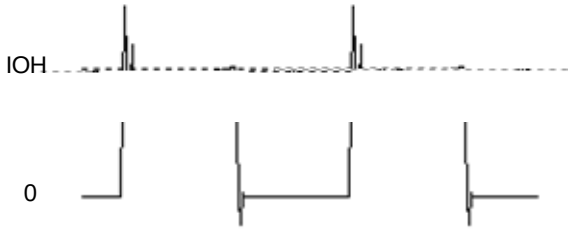
At this time, use a device for the open collector driver that

The motor current, I_{OH}, is set using the Pin 19 voltage, Vref, of the IPM.
Equations related to I_{OH} and Vref are given below.

Vref (RO2 (RO2+RO1)) V_{DD}(5 V) ····· (1)

I_{OH} (Vref 4.9) Rs ····· (2)

The value of 4.9 in Equation (2) above represents the Vref voltage as divided by a circuit inside the control IC.
Rs : 0.141 (Current detection resistor inside the IPM)



[Smoke Emission Precuations]
If Pin 18 (S.G terminal) is attached to the board without using solder, overcurrent may flow into the MOSFET at V_{CC}ON (24 V ON), causing the STK672-732AN-E to emit smoke because 5 V circuits cannot be controlled.

Input Pin Functions

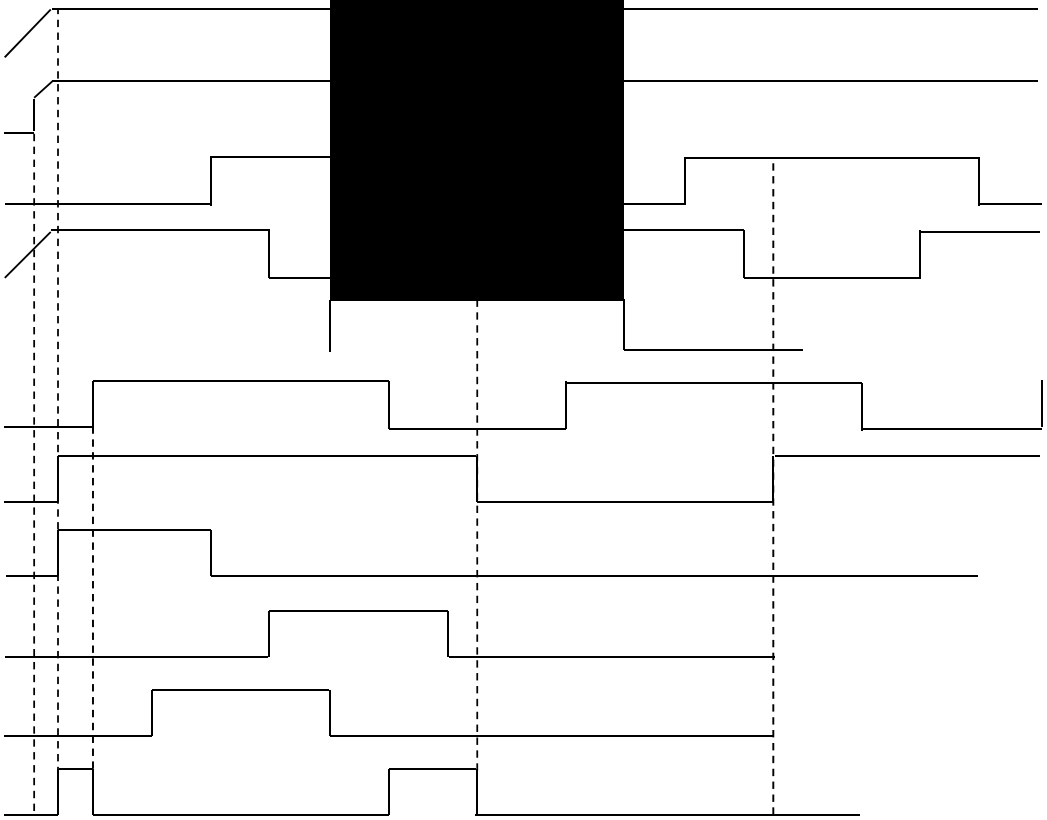
Pin Name	Pin No.	Function	Input Conditions When Operating
ΦA	13	Phase signal input of 5pin (phase A output).	Low active(with a function to prevent simultaneous ON of ΦA and ΦAB ,or ΦB and ΦBB.
ΦAB	17	Phase signal input of 7pin (phase AB output).	
ΦB	12	Phase signal input of 3pin (phase B output).	
ΦBB	10	Phase signal input of 1pin (phase BB output).	
RESETB	14	System reset Initial state of A and BB phase excitation in the timing charts is set by switching from low to high.	A reset is applied by a low level
ENABLE	15	The A, AB, B, and BB outputs are turned off, and after operation is restored by returning the ENABLE pin to the high level, operation continues with the same excitation timing as before the low-level input.	The A, AB, B, and BB outputs are turned off by a low-level input.

Output Pin Functions

Pin Name	Pin No.	Function	Input Conditions When Operating
FAULT	16	Monitor pin used when over-current detection or overheat detection function is activated.	Low level is output when detected.

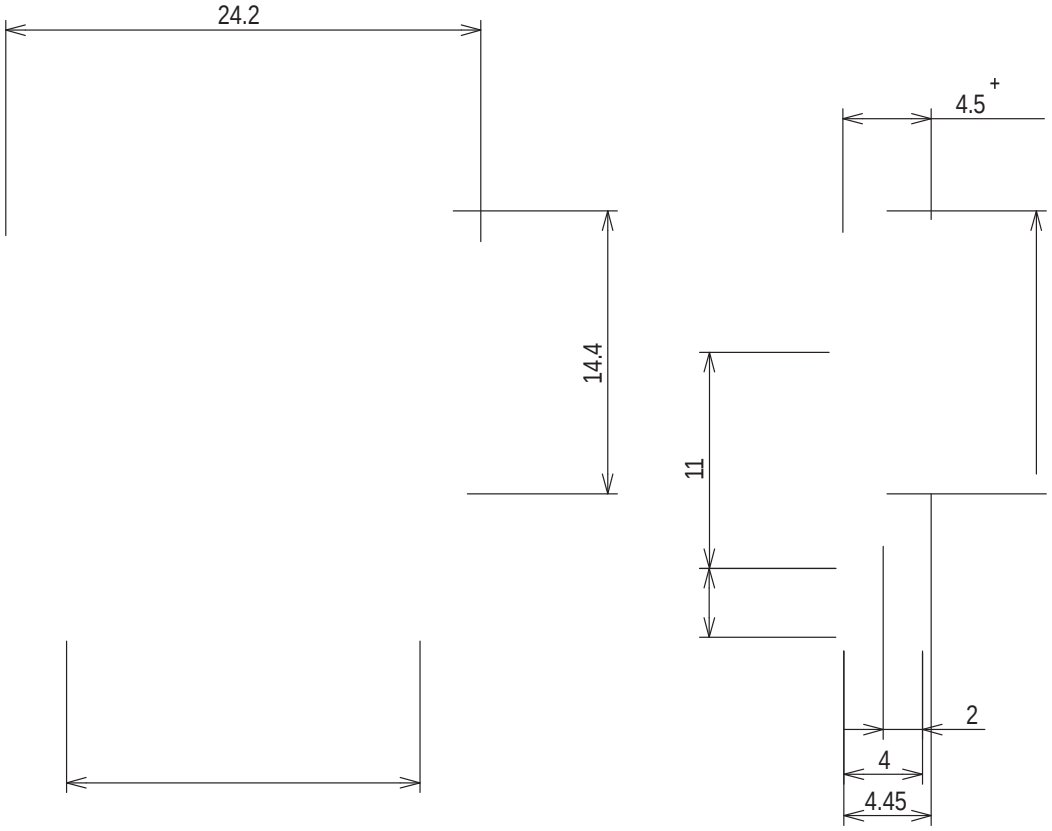
Note : See the timing chart for the concrete details on circuit operation.

1-2 phase excitation (ENABLE)



PACKAGE DIMENSIONS
unit : mm

SIP19 24.2x14.4
CASE 127BA
ISSUE O



STK672-732AN-E
Technical data

1. Input Pins and Functional Overview
2. STK672-732AN-E over current detection, thermal shutdown detection.
3. STK672-732AN-E Allowable Avalanche Energy
4. STK672-732AN-E Internal Loss Calculation
5. Thermal Design
6. Package Power Loss PdPK Derating Curve for the Ambient Temperature Ta
7. Example of Stepper Motor Driver Outp

1. I/O Pins and Functions of the Control Block

[Pin description]

IPM pin	Pin Name	Function
14	RESETB	System reset
15	ENABLE	Motor current OFF
16	FAULT	Overcurrent/over-heat detection output
19	Vref	Current value setting

Description of each pin

1-1.[RESETB (System-wide reset)]

The reset signal is formed by the power-on reset function built into the IPM and the RESETB terminal.

When activating the internal circuits of the IPM using the power-on reset signal within the IPM, be sure to connect Pin 14 of the IPM to V_{DD}.

1-5. [Input timing]

The control IC of the driver is equipped with a power on reset function capable of initializing internal IC operations when power is supplied. A 4 V typ setting is used for power on reset. Because the specification for the MOSFET gate voltage is 5 V 5%, conduction of current to output at the time of power on reset adds electromotive stress to the MOSFET due to lack of gate voltage. To prevent electromotive stress, be sure to set ENABLE = Low while V_{DD}, which is outside the operating supply voltage, is less than 4.75 V.

RESETB, ENABLE, A to BB Signals Input Timing

1-6. [Configuration of control block I/O pins]

<Configuration of the A, AB, B, BB, ENABLE, and RESETB input pins>

Input pins 13,17,12,10,15,14pin

(2) I_D and V_{DSS} Operating Waveforms in Non-avalanche Mode

Although the waveforms during avalanche mode are given in Figure 1, sometimes an avalanche does not result during actual operations.

Factors causing avalanche are listed below.

Poor coupling of the motor's phase coils (electromagnetic coupling of A phase and AB phase, B phase and BB phase).

Increase in the lead inductance of the harness caused by the circuit pattern of the board and motor.

Increases in V_{DSS}, tAVL, and IAVL in Figure 1 due to an increase in the supply voltage from 24 V to 36 V.

If the factors above are negligible, the waveforms shown in Figure 1 become waveforms without avalanche as shown in Figure 2.

Under operations shown in Figure 2, avalanche does not occur and there is no need to consider the allowable loss range of PAVL shown in Figure 3.

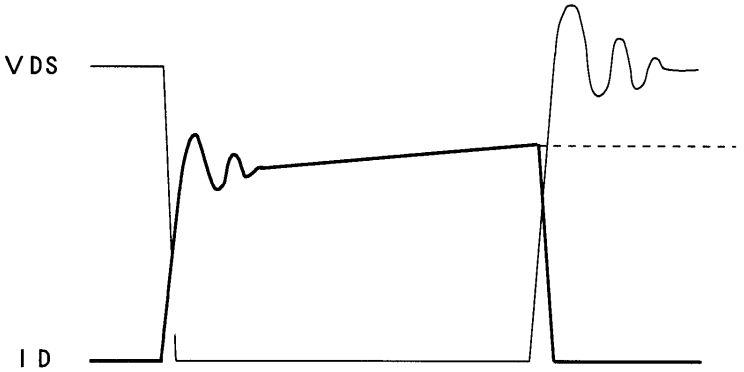
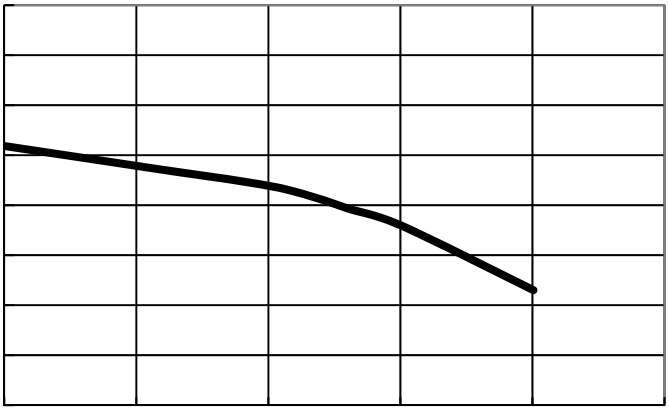


Figure 2. Output Current, I_D, and Voltage, V_{DS}, Waveforms 2 of the STK672-7** Series when Driving a 2-Phase Stepper Motor with Constant Current Chopping



4. Calculating STK672-732AN-E IPM Internal Power Loss

The average internal power loss in each excitation mode of the STK672-732AN-E can be calculated from the following formulas.

Each excitation mode
2-phase excitation mode
2PdAVex = (Vsat+Vdf) (1/(t1+t2+t3)) IOH t2+(1/(t1+t2+t3)) IOH (Vsat t1+Vdf t3)

1-2 Phase excitation mode
1-2PdAVex = (Vsat+Vdf) (1/(t1+t2+t3)) IOH t2+(1/(t1+t2+t3)) IOH (Vsat t1+Vdf t3)

Motor hold mode
HoldPdAVex = (Vsat+Vdf) I_{OH}

Vsat : Combined voltage represented by the Ron voltage drop+shunt resistor
Vdf : Combined voltage represented by the MOSFET body diode+shunt resistor

t1, t2, and t3 represent the waveforms shown in the figure below.

t1 : Time required for the winding current to reach the set current (I_{OH})
t2 : Time in the constant current control (PWM) region
t3 : Time from end of phase input signal until inverse current regeneration is complete

Motor COM Current Waveform Model

t1 = (-L/(R+0.33)) ln (1-(((R+0.33)/V_{CC}) I_{OH}))
t3 = (-L/R) ln ((V_{CC}+0.33)/(I_{OH} R+V_{CC}+0.33))
V_{CC} : Motor supply voltage (V)
L : Motor inductance (H)
R : Motor winding resistance ( )
I_{OH} : Motor set output current crest value (A)

For the values of Vsat and Vdf, be sure to substitute from Vsat vs I_{OH} and Vdf vs I_{OH} at the setting current value I_{OH}. (See pages to follow)
Then, determine if a heat sink is necessary by comparing with the Tc vs Pd graph (see next page) based on the calculated average output loss, IPM.
For heat sink design, be sure to see ‘5. Thermal Design’.
The IPM average power, PdAVex described above, represents loss when not in avalanche mode.

To add the loss in avalanche mode, be sure to add PAVL using the formula (for average power loss , PAVL, for u

4-2. [Calculating the average power loss, PAVL, during avalanche mode]

The allowable avalanche energy, EAVL, during fixed current chopping operation is represented by Equation (3-2) used to find the average power loss, PAVL, during avalanche mode that is calculated by multiplying Equation (3-1) by the chopping frequency.

$PAVL = V_{DSS}$ IAVL 0.5 tAVL fc ····· (3-2)

fc : Hz units (fc is set to the PWM frequency of 50kHz.)

Be sure to actually operate an STK672-7** series and substitute values found when observing operations on an oscilloscope for V_{DSS}, IAVL, and tAVL.

The sum of PAVL values for each excitation mode is multiplied by the constants given below and added to the average internal IPM loss equation, except in the case of 2-phase excitation.

1-2 excitation mode and higher : PAVL(1) = 0.7 PAVL ·····(4-1)

During2-phase excitation mode and motor hold : PAVL(1) = 1 PAVL ·····(4-2)

5. Thermal design

[Operating range in which a heat sink is not used]

Use of a heat sink to lower the operating substrate temperature of the IPM (Intelligent Power Module) is effective in increasing the quality of the IPM.

The size of heat sink for the IPM varies depending on the magnitude of the average power loss, PdAV, within the IPM. The value of PdAV increases as the output current increases. To calculate PdAV, refer to “Calculating Internal IPM Loss” in the specification document.

Calculate the internal IPM loss, PdAV, assuming repeat operation such as shown in Figure 1 below, since conduction during motor rotation and off time both exist during actual motor operations,

Figure 1. Motor Current Timing

T1 : Motor rotation operation time

T2 : Motor hold operation time

T3 : Motor current off time

T2 may be reduced, depending on the application.

T0 : Single repeated motor operating cycle

pe I_O1 a

Figure 2

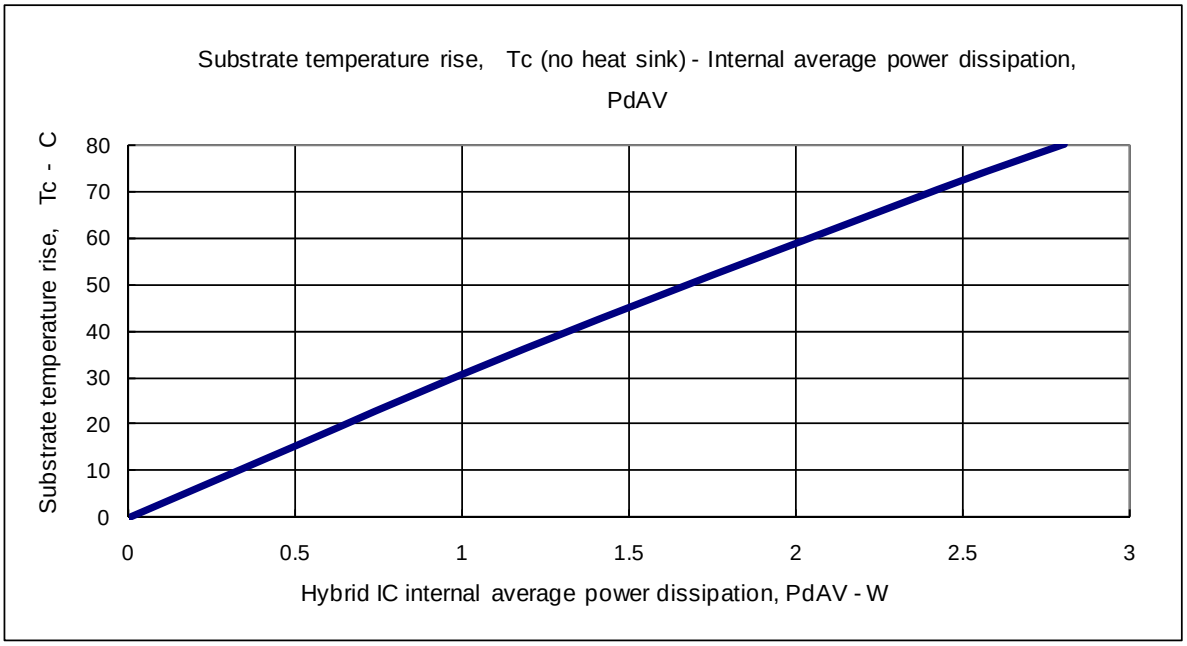
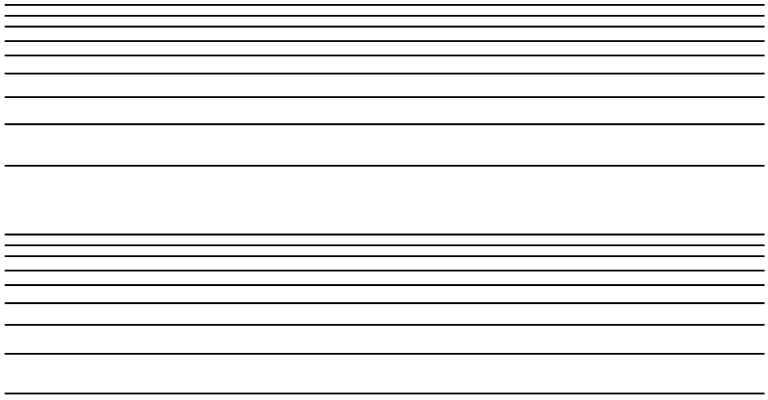
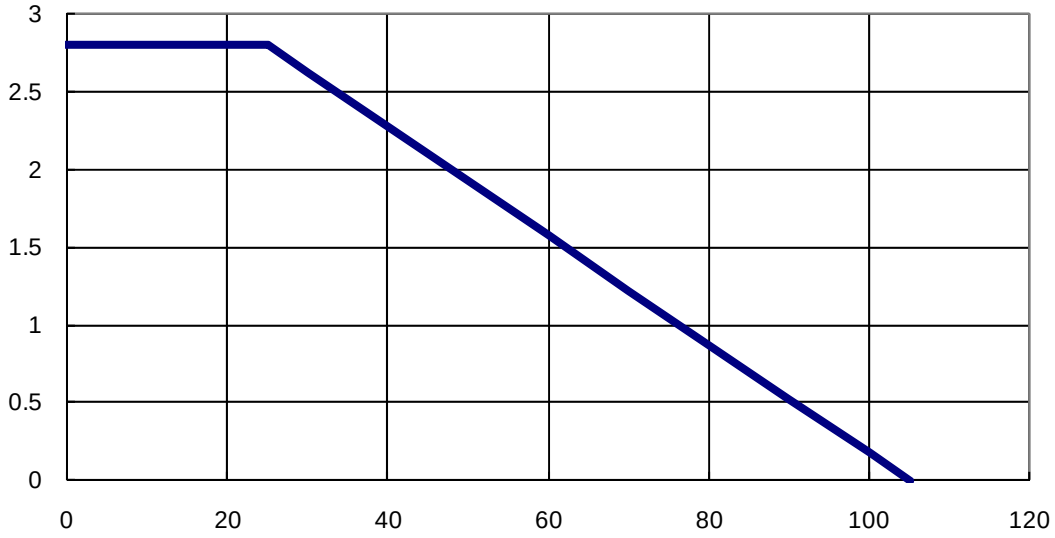


Figure 3



6. Mitigated Curve of Package Power Loss, PdPK, vs. Ambient Temperature, Ta

Package power loss, PdPK, refers to the average internal power loss, PdAV, allowable without a heat sink. The figure below represents the allowable power loss, PdPK, vs. fluctuations in the ambient temperature, Ta. Power loss of up to 2.8 W is allowable at Ta = 25 C, and of up to 1.5 W at Ta = 60 C.
* The package thermal resistance θc-a is 28.6°C/W.



(5) When mounting multiple drivers on a single board

When mounting multiple drivers on a single board, the GND design should mount a V_{CC} decoupling capacitor, C1, for each driver to stabilize the GND potential of the other drivers. The key wiring points are as follows.

(6) V_{CC} operating limit