

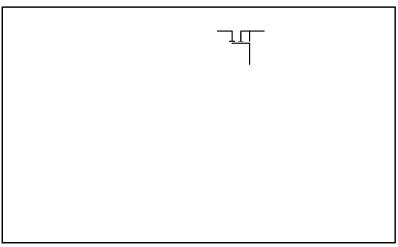
LDOR a - 1 A,
U a L D , CMOS,
B a Ra

Product Preview

T30LMPSR131, T30LAPSR131

The T30LxPSR131 is a 1 A LDO equipped with an NMOS pass transistor and a separate bias supply voltage (V

T30LMPSR131, T30LAPSR131



*Active output discharge function is present only in "A" and "C" option devices.

Figure 2. Simplified Schematic Block Diagram - Fixed Version

T30LMPSR131, T30LAPSR131

ELECTRICAL CHARACTERISTICS

 $(-40 \,^{\circ}\text{C} \le T_J \le 125 \,^{\circ}\text{C}; \, V_{BIAS} = 2.7 \,\text{V}$ or $(V_{OUT} + 1.6 \,\text{V})$, whichever is greater, $V_{IN} = V_{OUT(NOM)} + 0.1 \,\text{V}$, $I_{OUT} = 1 \,\text{mA}$, $V_{EN} = 1 \,\text{V}$, $C_{IN} = 4.7 \,\mu\text{F}$, $C_{OUT} = 10 \,\mu\text{F}$, $C_{BIAS} = 1 \,\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25 \,^{\circ}\text{C}$. Min/Max values are for $-40 \,^{\circ}\text{C} \le T_J \le 125 \,^{\circ}\text{C}$ unless otherwise noted. (Note 4))

Parameter	Test Conditions	Symbol	Min	Тур	Max	Unit
Operating Input Voltage Range		V_{IN}	$V_{OUT} + V_{DO}$		2.2	V
Operating Bias Voltage Range		V _{BIAS}	(V _{OUT} +			

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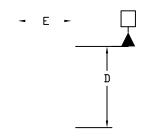
ELECTRICAL CHARACTERISTICS (continued)

 $(-40 \,^{\circ}\text{C} \le T_J \le 125 \,^{\circ}\text{C}; \, V_{BIAS} = 2.7 \,\text{V} \,\text{or} \, (V_{OUT} + 1.6 \,\text{V}), \, \text{whichever is greater}, \, V_{IN} = V_{OUT(NOM)} + 0.1 \,\text{V}, \, I_{OUT} = 1 \,\text{mA}, \, V_{EN} = 1 \,\text{V}, \, C_{IN} = 4.7 \,\mu\text{F}, \, C_{OUT} = 10 \,\mu\text{F}, \, C_{BIAS} = 1 \,\mu\text{F}, \, \text{unless otherwise noted}.$ Typical values are at $T_J = +25 \,^{\circ}\text{C}$. Min/Max values are for $-40 \,^{\circ}\text{C} \le T_J \le 125 \,^{\circ}\text{C}$ unless otherwise noted. (Note 4))

Parameter Min7o6S Тур Max Unit

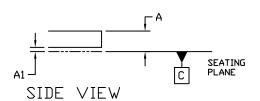
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DATE 29 JAN 2020



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3. COPLANARITY APPLIES TO THE SPHERICAL



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DIM	MIN.	N□M.	
Α			
A1	0.04	0.06	
A2			
D			
·			
e	0.400 BSC		

BOTTOM VIEW

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