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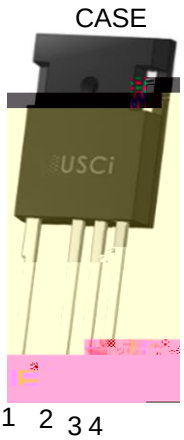
DATASHEET

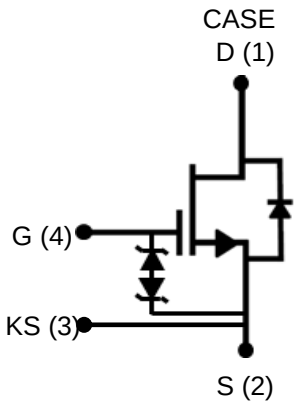
UF3C065030K4S

Rev. , January 20‰Œ

Description

United Silicon Carbide's cascode products co-package its high-performance F3 SiC fast JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits very fast switching using a 4-terminal TO-247-package and the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.





Features

Part Number	Package	Marking
UF3C065030K4S	TO-247-4L	UF3C065030K4S

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

		Min	Typ	Max	
	BV_{DS}	650			V
			6	150	
			30		
	I_{GSS}		6	20	μA
			27	35	
			43		
	V				

Typical Performance - Dynamic

	Min	Typ	Max

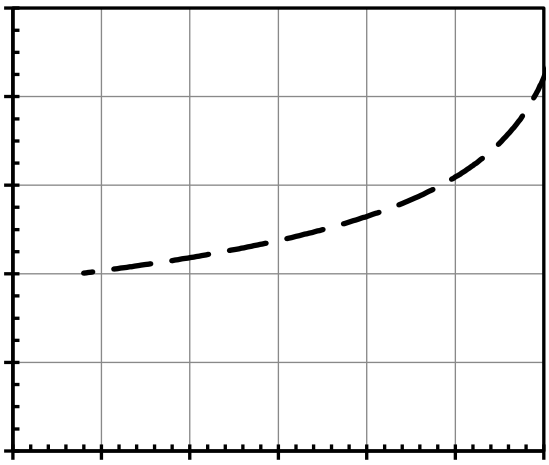


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V

Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

Figure 8. Typical gate charge at V_{DS} = 400V and I_D = 50A

Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

Figure 14. DC drain current derating

Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance

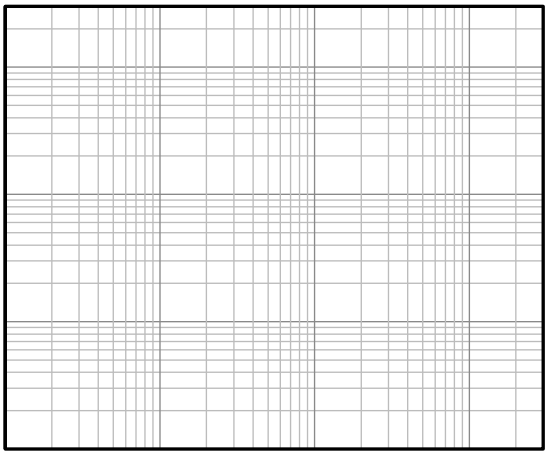


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

Figure 18. Clamped inductive switching energy vs. drain current at T_J = 25°C

Figure 19. Clamped inductive switching turn-on energy vs. R_{G,EXT_ON}

Figure 20. Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

Figure 21. Clamped inductive switching energy vs. junction temperature at V_{DS} = 400V and I_D = 50A

Figure 22. Reverse recovery charge Qrr vs. junction temperature

Applications Information

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in seri4 (o)-5 (wehTJ 0 -11.78 Tn( )-3TJ 0 - h06 (

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see www.unitedsic.com.

Disclaimer

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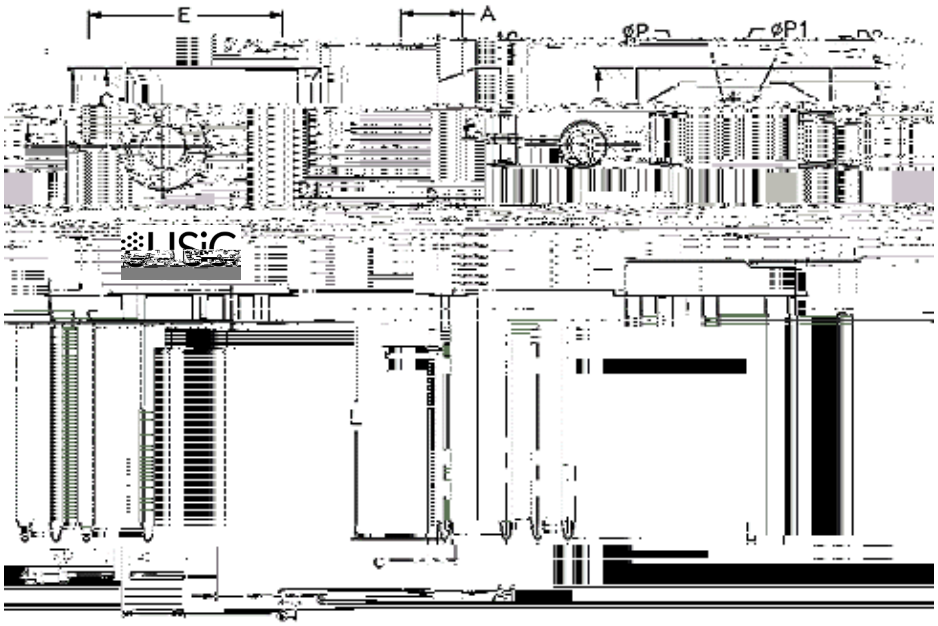
TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PACKAGE OUTLINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
ΦP				
ΦP1				

TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PART MARKING

PACKING TYPE