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DATASHEET

UF3C065040K4S



Rev. , January ‰ ‡ ‰ Œ

Description

CASE G(4) KS(3) S(2)G(2)

Part Number	Package	Marking
UF3C065040K4S	TO-247-4L	UF3C065040K4S



United Silicon Carbide's cascode products co-package its highperformance F3 SiCfast JFETs with acascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits very fast switching using a4-terminal TO-247package and the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.

Features

Š Typical on-resistance $R_{DS(on),typ}$ of 42m : Š

Typical applications

- ŠEV charging
- ŠPV inverters
- Š Switch mode power supplies
- Š Power factor correction modules
- Š Motor drives
- Š Induction heating





Maximum Ratings

	Symbol		Value	Units
	V _{DS}		650	V
Gate-source voltage	V _{GS}	DC	-25 to +25	V
			54	Α
			40	А
	I _{DM}		125	А
	E _{AS}		76	mJ
	P _{tot}		326	W
	$T_{J,max}$		175	°C
	T _J , T _{STG}		-55 to 175	°C
Max. lead temperature for soldering,	TL		250	°C

- 1. Limited by $T_{\text{J,max}}$
- 2. Pulse width t_p limited by $T_{J,max}$
- 3. Starting $T_J = 25^{\circ}C$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Unite
			Min	Тур	Max	Units
Thermal resistance, junction-to-case	R_{T}			0.35	0.46	°C/W





Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

		Min	Тур	Max	
	BV _{DS}	650			V
			0.7	150	
			10		
	I _{GSS}		6	20	FA
Drain-source on-resistance			42	52	
			78		
	V _{G(th)}	4	5	6	V
	R _G		4.5		:

Typical Performance - Reverse Diode

			Min	Тур	Max	
	I _S				54	А
	I _{S,pulse}				125	А
				1.5	1.75	
				1.8		
Reverse recovery charge	Q _{rr}	V _R =400V, I _F =40A, V _{GS} =-5V, R _{G_EXT} =20 :		138		nC
Reverse recovery time	t _{rr}	di/dt=1100A/ Bs, Tj=25°C		38		ns
Reverse recovery charge	Q _{rr}	V _R =400V, I _F =40A, V _{GS} =-5V, R _{G_EXT} =20 :		137		nC
Reverse recovery time	t _{rr}	$T_{J}=150^{\circ}C$		38		ns





Typical Performance - Dynamic

Min Тур Max





Learn More

Contr







- Figure 1. Typical output characteristics at $T_J = -55^{\circ}$ C, tp < 250 B
- Figure 2. Typical output characteristics at T_{J} = 25°C, tp < 250 $\ensuremath{\mathbb{R}}$

Figure 3. Typical output characteristics at $T_J = 175^{\circ}C$, tp < 250 B

Figure 4. Normalized on-resistance vs. temperature at $V_{GS}\,{=}\,12V$ and $I_{D}\,{=}\,40A$



Figure 9. 3rd quadrant characteristics at $T_J = -55^{\circ}C$

Figure 10. 3rd quadrant characteristics at $T_J = 25^{\circ}C$

Figure 11. 3rd quadrant characteristics at $T_J = 175^{\circ}C$

Figure 12. Typical stored energy in
$$C_{OSS}$$
 at $V_{GS} = 0V$









Figure 13. Typical capacitances at f = 100 kHz and $V_{GS} = 0V$

Figure 14. DC drain current derating















Figure 21. Clamped inductive switching energy vs. junction temperature at V $_{DS}$ = 400V and I $_{D}$ = 40A

Applications Information

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{ass}), gate charge (Q), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see www.unitedsic.com.

Disclaimer

United Silicon Carbide, Inc. reserves the right to change or modify any of the products and their inherent physical and technical specifications without prior notice. United Silicon Carbide, Inc. assumes no responsibility or liability for any errors or inaccuracies within. Figure 22. Reverse recovery charge Qrr vs. junction temperature

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TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PACKAGE OUTLINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
Р				
P1				



TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PACKING TYPE

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