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Maximum Ratings

Symbol	Value	Units
V _{DS}	650	V
V _{GS}	-25 to +25	V
	54	А
	40	А
I _{DM}	125	А
E _{AS}	76	









Electrical Characteristics (T_J





Typical Performance - Dynamic

	C _{iss} C _{oss} C _{rss}		Min	Тур 1500 200 2.2	Max	
	$C_{\text{oss(er)}}$			146		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V _{DS} =0V to 400V, V _{GS} =0V		325		pF
C _{oss}	E _{oss}			11.7		ß
Total gate charge	Q _G	V _{DS} =400V, I _D =40A,		51		-
Gate-drain charge	Q _{GD}	$V_{GS} = -5V \text{ to} 15V$		11		nC
Gate-source charge	Q _{GS}			19 35		
	t _{d(on)} t _r			24		
				57		
	t _{d(off)} t _f			14		
	E _{ON}			500		
	E _{OFF}			118		
Total switching energy including $R_{\!S}$ energy ⁴	E _{TOTAL}			618		
Snubber R _s energy during turn-on	E _{RS_ON}			1.7		
Snubber R_s energy during turn-off	E _{RS_OFF}			4.5		
Turn-on delay time	t _{d(on)}			35		
Rise time	t _r	V _{DS} =400V, I _D =40A, Gate		22		
Turn-off delay time	t _{d(off)}	Driver =-5V to +15V,		60		ns
Fall time	t _f	Turn-on R _{G,EXT} =1.8 : ,		13		
Turn-on energy including $P_S energy^4$	E _{ON}	Turn-off R _{G,EXT} =22 : Inductive Load,		479		
Turn-off energy including $R_S energy^4$	E _{OFF}	FWD: same device with		124		
Total switching energy including $R_{\!S}$ energy ⁴	E _{TOTAL}	V_{GS} = -5V and R_{S} = 22 : , RC snubber: R_{S} =5 : and		603		ß
Snubber P_S energy during turn-on	E_{RS}	С _S =150рF, Т _J =150°С		1.8		
Snubber R_s energy during turn-off	E_{RS}_{OFF}			5.3		

4. The switching performance are evaluated with a RC snubber circuit as shown in Figure 24.

















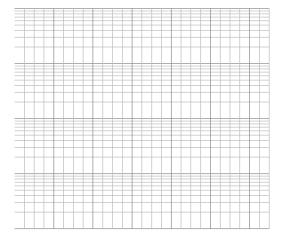


Figure 13. Typical capacitances at f = 100kHz and & = 0V

Figure 14. DC drain current derating

Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance



















D O N

(a)

(b)

(a)

(b)









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(a) (b) Figure 22. Clamped inductive switching energy including RC snubber energy loss (a) and RC snubber energy I

(a)

(b)









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Figure 24. Clamped inductive load switching test circuit An RC snubber ($R_s = 5$: and $C_s = 150$ pF) is required to improve the turn-off waveforms.

Applications Information

SiC FETs are enhancement-mode power switches formed by a highvoltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{ss}

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

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TO-220-3L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PART MARKING

PACKING TYPE

ANTI-STATIC TUBE

QUANTITY /TUBE : 50 UNITS

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