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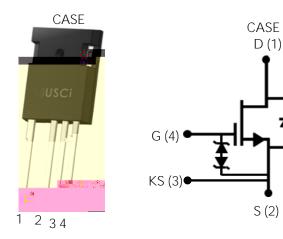






DATASHEET

UF3C065080K4S



Part Number	Package	Marking
UF3C065080K4S	TO-247-4L	UF3C065080K4S







Maximum Ratings

Parameter		Symbol	Test Conditions	5	Value	Units
Drain-source voltage		V _{DS}			650	V
Gate-source voltage		V _{GS}	DC		-25 to +25	V
Continuous drain current ¹		Ι _D	$T_{\rm C} = 25^{\circ}{\rm C}$ $T_{\rm C} = 100^{\circ}{\rm C}$		31 23	A A
Pulsed drain current ²		I _{DM}	$T_{\rm C} = 25^{\circ}{\rm C}$		65	A
Single pulsed avalanche energy 3		E _{AS}	L=15mH, I _{AS} =2	.1A	33	mJ
Power dissipation		P _{tot}	$T_{\rm C} = 25^{\circ}{\rm C}$		190	W
Maximum junction temperature		T _{J,max}			175	°C
Operating and storage temperature		T _J , T _{STG}			-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds		TL			250	°C
1. Limited by $T_{J,max}$ 2. Pulse width t_p limited by $T_{J,max}$ -3. Starting $T_J = 25^{\circ}C$						
Thermal Characteristics						
Parameter	Symbol	Test Conditions		Value	_	Units
			Min	Тур	Max	
Thermal resistance, junction-to-case	R_q			0.61	0.79	°C/W





Electrical Characteristics ($T_J = +25^{\circ}Cunless \text{ otherwise specified}$)

Typical Performance - Static

BV _{DS}	Min 650	Тур	Max	V
		6	100	
		40		
I _{GSS}		6		





Typical Performance - Dynamic

	C _{iss} C _{oss} C _{rss}		Min	Typ 1500 104 2.6	Max	_
	C _{oss(er)}			77		pF
	C _{oss(tr)}			176		pF
	E _{oss}			6.2		mJ
Total gate charge	Q_G	V _{DS} =400V, I _D =20A,		43		
Gate-drain charge	Q _{GD}	$V_{GS} = -5V \text{ to } 12V$		11		nC
Gate-source charge	Q _{GS}			19		
	t _{d(on)}			21		
	t _r			20		
	t _{d(off)}			37		
	t _f			8		
	E _{ON}			121		
	E _{OFF}			41		
Total switching energy	E _{TOTAL}			162		
Turn-on delay time	t _{d(on)}	V_{DS} =400V, I_{D} =20A,		17		
	t _r	Gate Driver =-5V to		18		
	t _{d(off)}	+12V, Turn-on R _{G,EXT} =8.5W,		36		
	t _f	Turn-off $R_{G,EXT}$ =20W		7		
	E _{ON}	Inductive Load,		107		
	E _{OFF}	FWD: same device with		31		
	E _{total}	$V_{GS} = -5V, R_{G} = 10W$		138		
	-TUTAL			100		









Typical Performance Diagrams

Figure 1. Typical output characteristics at T_J = -55°C, tp < 250ms

Figure 2. Typical output characteristics at $T_J = 25^{\circ}C$, tp < 250ms

Figure 3. Typical output characteristics at $T_J = 175$ °C, tp < 250ms

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 20A





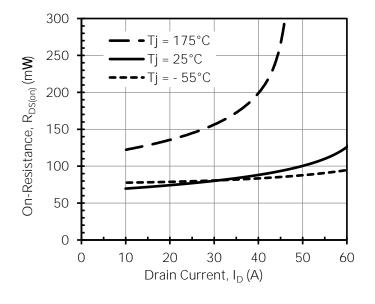


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

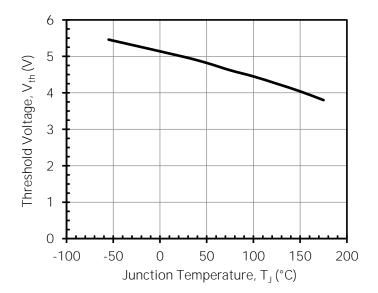


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_{D} = 10mA

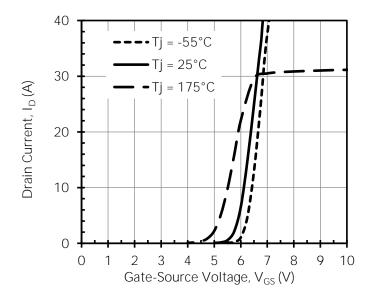


Figure 6. Typical transfer characteristics at V_{DS} = 5V

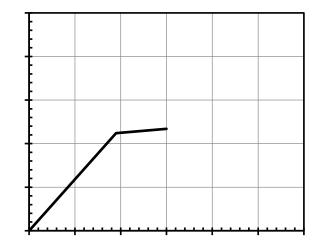


Figure 8. Typical gate charge at V_{DS} = 400V and I_{D} = 20A











Figure 9.	3rd	quadrant	characteristics	at T _J	= -55°C
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Figure 10. 3rd quadrant characteristics at $T_J = 25^{\circ}C$

Figure 11. 3rd quadrant characteristics at $T_J = 175^{\circ}C$ Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0V$





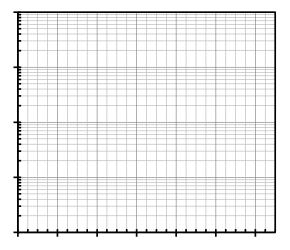


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

Figure 14. DC drain c	current derating
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Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance





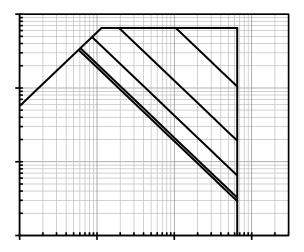


Figure 17. Safe operation area at T_{C} = 25°C, D = 0, Parameter t_{p}

Figure 18. Clamped inductive switching energy vs. drain current at $T_{\rm J}$ = 25 $^{\circ}{\rm C}$

Figure 19. Clamped inductive switching turn-on energy vs. $R_{G,\text{EXT}_\text{ON}}$

Figure 20. Clamped inductive switching turn-off energy vs. $R_{G,\text{EXT_OFF}}$









Figure 21. Clamped inductive switching energy vs. junction temperature at V_{DS} = 400V and I_{D} = 20A

Applications Information

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see www.unitedsic.com.

Disclaimer

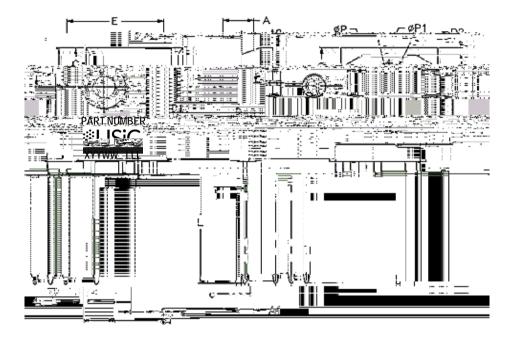
United Silicon Carbide, Inc. reserves the right to change or modify any of the products and their inherent physical and technical specifications without prior notice. United Silicon Carbide, Inc. assumes no responsibility or liability for any errors or inaccuracies within. Figure 22. Reverse recovery charge Qrr vs. junction temperature

United Silicon Carbide, Inc. assumes no liability whatsoever relating to the choice, selection or use of the United Silicon Carbide, Inc. products and services described herein.



TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PACKAGE OUTLINE



DIM	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	
P P1					



TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PACKING TYPE

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