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DATASHEET

UF3C120040K4S

Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TO-247-4L, 1200 V, 35 mohm

Rev. B, Jan 2025

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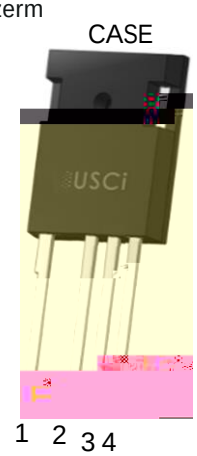

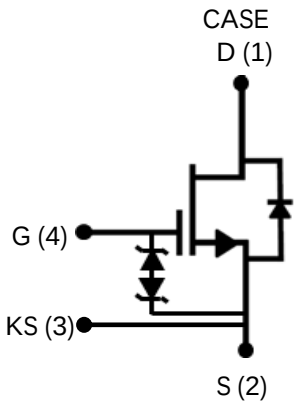

Part Number	Package	Marking
UF3C120040K4S	TO-247-4L	UF3C120040K4S

Description

United Silicon Carbide's cascode products co-package its high-performance F3 SiC fast JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits very fast switching tha S09 0 Td(3)4

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C = 25°C	65	A
		T_C = 100°C	47	A
Pulsed drain current [2]	I_{DM}	T_C = 25°C	175	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =4.2A	132.3	mJ
Power dissipation	P_{tot}	T_C = 25°C	429	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, Fv?uol1-v;ouv1om7v	T_L		250	°C

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	R_q			0.27	0.35	°C/W

Electrical Characteristics

Typical Performance - Static

	Min	Typ	Max	
BV_{DS}	1200			V
		8	150	
		35		
I_{GSS}		6	20	mA
		35	45	
		73		
$V_{G(th)}$	4	5	6	V
R_G		4.5		W

Typical Performance - Reverse Diode

	Min	Typ	Max
I_S			65

Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V

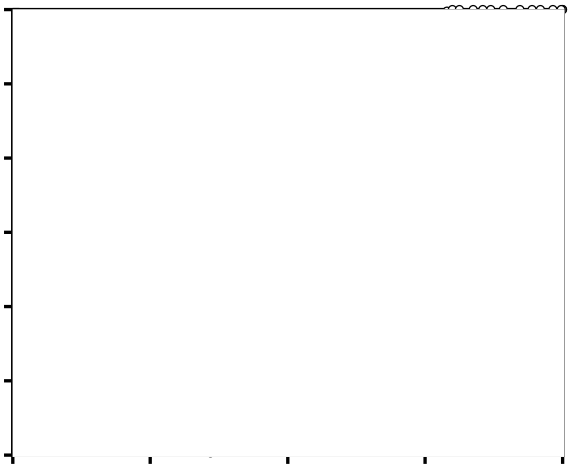

Figure 9. 3rd quadrant characteristics at T_J = -55°C

Figure 10. 3rd quadrant characteristics at T_J = 25°C

Figure 11. 3rd quadrant characteristics at T_J = 175°C

Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

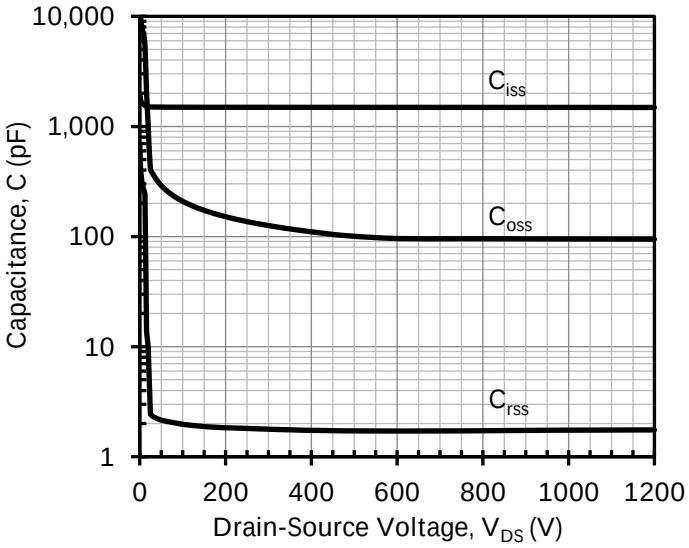

Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

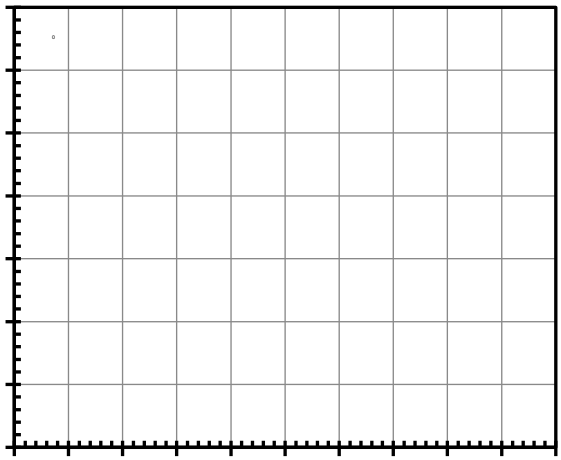

Figure 14. DC drain current derating

Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance

Figure 17. Safe operation area at T_C = 25°C, D = 0,
Parameter t_p

Figure 22. Reverse recovery charge Qrr vs. junction temperature

Applications Information

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see www.unitedsic.com.

Disclaimer

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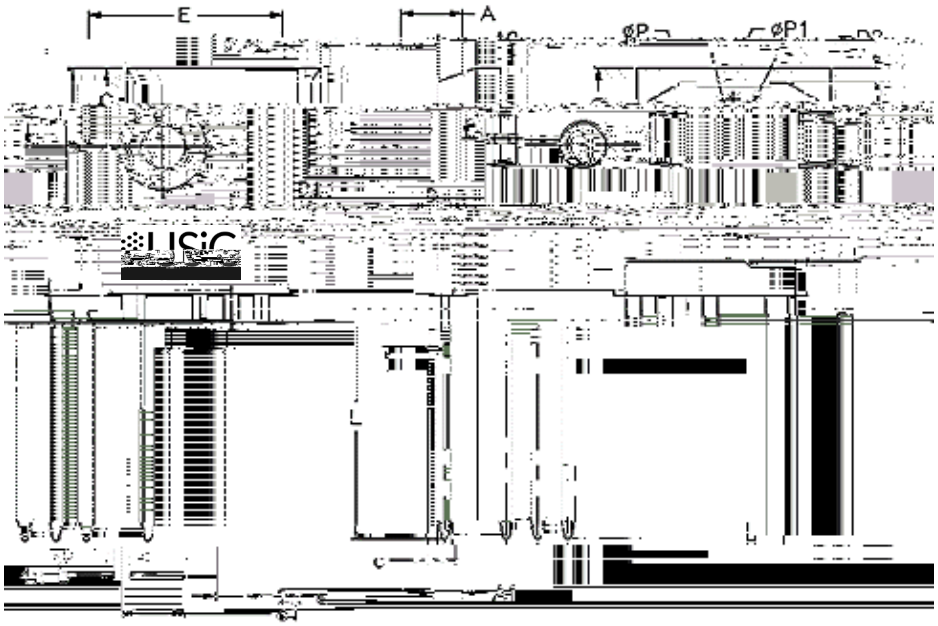
TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PACKAGE OUTLINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
ΦP				
ΦP1				

TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PART MARKING

PACKING TYPE