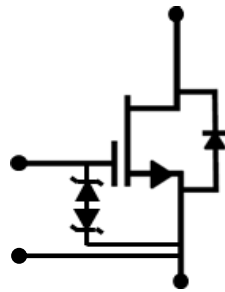
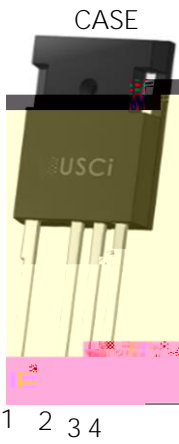


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Part Number	Package	Marking
UF3C120080K4S	TO-247-4L	UF3C120080K4S





Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current ¹	I_D	$T_C = 25^\circ\text{C}$	33	A
Pulsed drain current ²	I_{DM}	$T_C = 100^\circ\text{C}$	24	A
Single pulsed avalanche energy ³	E_{AS}	$T_C = 25^\circ\text{C}$	77	A
Power dissipation	P_{tot}	$L=15\text{mH}, I_{AS}=2.8\text{A}$	58.5	mJ
Maximum junction temperature	$T_{J,max}$	$T_C = 25^\circ\text{C}$	254.2	W
Operating and storage temperature	T_J, T_{STG}		175	$^\circ\text{C}$
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		-55 to 175	$^\circ\text{C}$
			250	$^\circ\text{C}$

1. Limited by $T_{J,max}$

2. Pulse width t_p limited by $T_{J,max}$

3. Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	R_q			0.45	0.59	$^\circ\text{C}/\text{W}$



Electrical Characteristics

Typical Performance - Static

	Min	Typ	Max	
BV_{DS}	1200			V
		10	75	
		50		
I_{GSS}		6	20	mA
		80	100	
		172		
$V_{G(th)}$	4	5	6	V
R_G		4.5		W

Typical Performance - Reverse Diode

	Min	Typ	Max	
I_S			33	A
$I_{S,puin}$				



Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=100V, V_{GS}=0V$ $f=100kHz$		1500		pF
Output capacitance	C_{oss}			100		
Reverse transfer capacitance	C_{rss}			2.1		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 800V, $V_{GS}=0V$		59		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 800V, $V_{GS}=0V$		136		pF
C_{oss} stored energy	E_{oss}	$V_{DS}=800V, V_{GS}=0V$		19		mJ
Total gate charge	Q_G	$V_{DS}=800V, I_D=20A,$ $V_{GS} = -5V$ to 12V		43		nC
Gate-drain charge	Q_{GD}			11		
Gate-source charge	Q_{GS}			19		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=800V, I_D=20A,$ Gate Driver = -5V to +12V, Turn-on $R_{G,EXT}=8.5W,$ Turn-off $R_{G,EXT}=20W$ Inductive Load, FWD: same device with $V_{GS} = -5V, R_G = 10W,$ $T_J=25^\circ C$		33		ns
Rise time	t_r			13		
Turn-off delay time	$t_{d(off)}$			43		
Fall time	t_f			10		
Turn-on energy	E_{ON}	FWD: same device with $V_{GS} = -5V, R_G = 10W,$ $T_J=25^\circ C$		355		mJ
Turn-off energy	E_{OFF}			88		
Total switching energy	E_{TOTAL}			443		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=800V, I_D=20A,$ Gate Driver = -5V to +12V, Turn-on $R_{G,EXT}=8.5W,$ Turn-off $R_{G,EXT}=20W$ Inductive Load, FWD: same device with $V_{GS} = -5V, R_G = 10W,$ $T_J=150^\circ C$		29		ns
Rise time	t_r			11		
Turn-off delay time	$t_{d(off)}$			45		
Fall time	t_f			10		
Turn-on energy	E_{ON}	FWD: same device with $V_{GS} = -5V, R_G = 10W,$ $T_J=150^\circ C$		306		mJ
Turn-off energy	E_{OFF}			82		
Total switching energy	E_{TOTAL}			388		



Typical Performance Diagrams

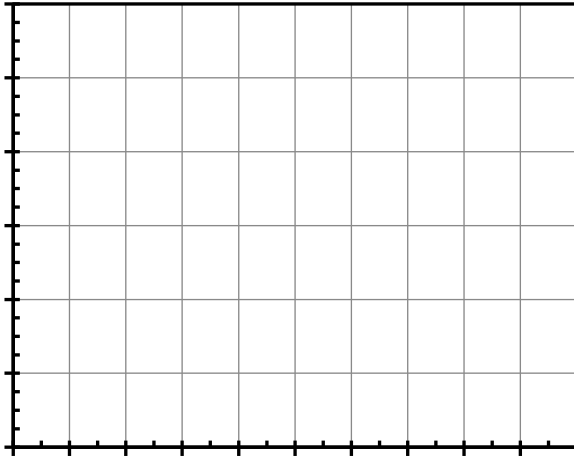


Figure 1. Typical output characteristics at $T_J = -55^\circ\text{C}$, $t_p < 250\text{ms}$

Figure 2. Typical output characteristics at $T_J = 25^\circ\text{C}$, $t_p < 250\text{ms}$

Figure 3. Typical output characteristics at $T_J = 175^\circ\text{C}$, $t_p < 250\text{ms}$

Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 20\text{A}$



Figure 5. Typical drain-source on-resistances at $V_{GS} = 12V$

Figure 6. Typical transfer characteristics at V_{DS}

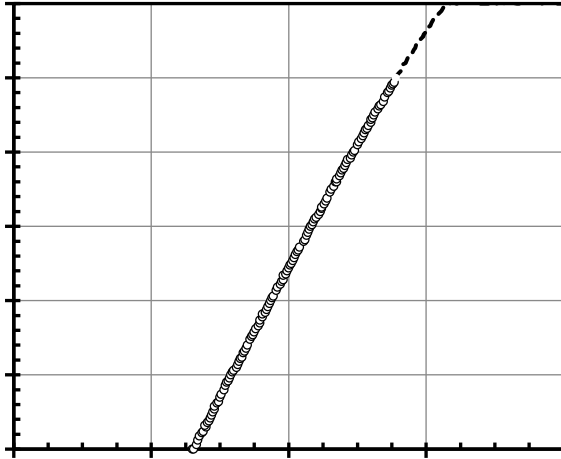


Figure 9. 3rd quadrant characteristics at $T_J = -55^\circ\text{C}$

Figure 10. 3rd quadrant characteristics at $T_J = 25^\circ\text{C}$

Figure 11. 3rd quadrant characteristics at $T_J = 175^\circ\text{C}$

Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$





Figure 22. Reverse recovery charge Q_{rr} vs. junction temperature

Applications Information

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see www.unitedsic.com.

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