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Typical Performance - Dynamic

	Min	Typ	Max	
C_{iss}		739		
C_{oss}		14.8		
C_{rss}		2		
$C_{oss(er)}$		17.5		pF
$C_{oss(tr)}$		36		pF
E_{oss}		5.6		nJ
Q_G		22.5		nC
Q_{GD}		6		nC
Q_{GS}		5.5		nC
$t_{d(on)}$		34		ns
t_r		10		ns
$t_{d(off)}$		33		ns
t_f		25		ns
E_{ON}		70		nJ
E_{OFF}				nJ



Typical Performance Diagrams

Figure 1. Typical output characteristics at $T_J = -55^\circ\text{C}$,
 $t_p < 250 \text{ ns}$

Figure 2. Typical output characteristics at $T_J = 25^\circ\text{C}$,
 $t_p < 250 \text{ ns}$

Figure 3. Typical output characteristics at $T_J = 175^\circ\text{C}$,
 $t_p < 250 \text{ ns}$



Figure 5. Typical drain-source on-resistances at $V_{GS} = 12V$

Figure 6. Typical transfer characteristics at $V_{DS} = 5V$

Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and I_D

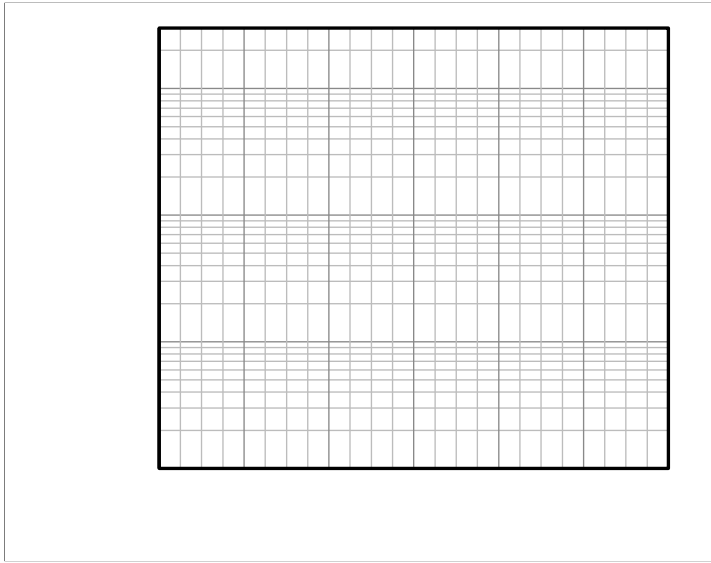


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{ds} = 0\text{V}$

Figure 14. DC drain current derating

Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance

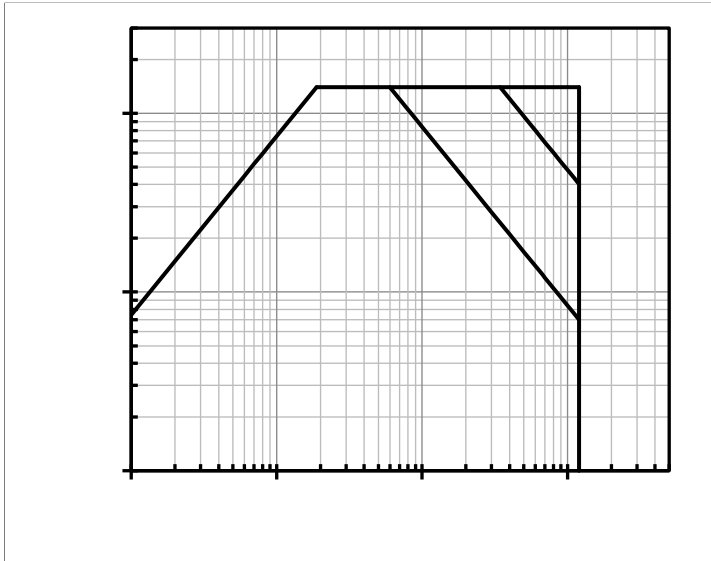


Figure 17. Safe operation area at $T_J = 25^\circ\text{C}$, $D = 0$, Parameter t_p

Figure 18. Reverse recovery charge Q_{rr} vs. junction temperature

Figure 19. Clamped inductive switching energy vs. drain current at $V_{DS} = 800\text{V}$ and $T_J = 25^\circ\text{C}$

Figure 20. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 800\text{V}$ and $I_D = 5\text{A}$



Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_g), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high



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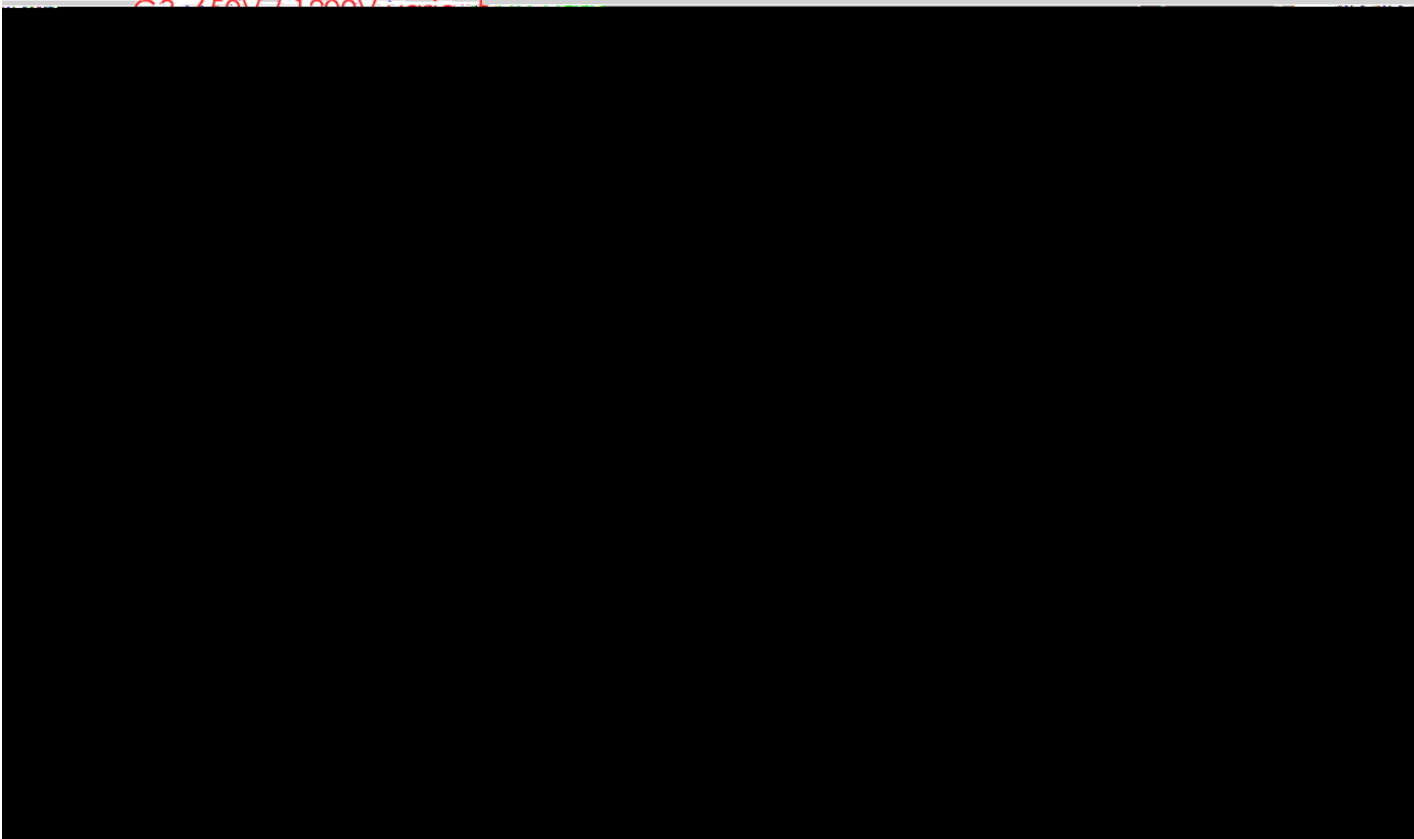
TO263-7L (D2PAK-7L) PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION

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
Rev D

PART MARKING



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