‰÷ C r ‰ *f*

. . ..

Typical Performance - Dynamic

	Min	Typ	Max	
C_{iss}		739		
C_{oss}		14.8		
C_{rss}		2		
$C_{oss(er)}$		17.5		pF
$C_{oss(tr)}$		36		pF
E_{oss}		5.6		μJ
Q_G		22.5		
Q_{GD}		6		
Q_{GS}		5.5		
$t_{d(on)}$		34		
t_r		10		
$t_{d(off)}$		33		
t_f		25		
E_{ON}		70		
E_{OFF}				

Typical Performance Diagrams

Figure 1. Typical output characteristics at T_j = - 55°C, tp < 250 µs

Figure 2. Typical output characteristics at T_j = 25°C, tp < 250 µs

Figure 3. Typical output characteristics at T_j = 175°C, tp < 250 µs

Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V

Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D

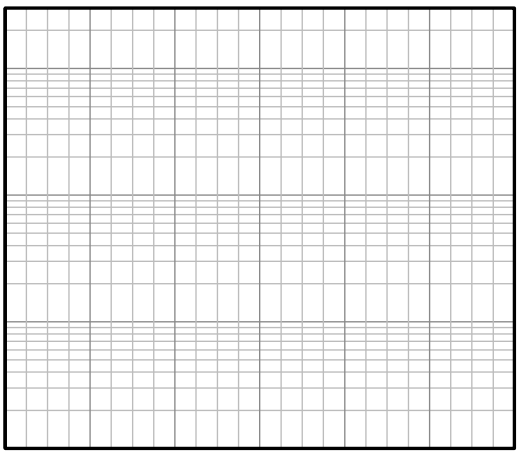

Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

Figure 14. DC drain current derating

Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance

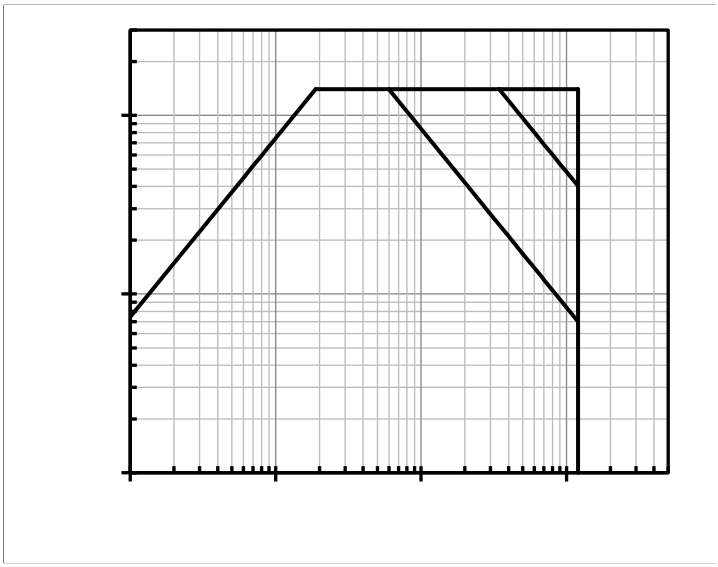

Figure 17. Safe operation area at T_c = 25°C, D = 0, Parameter t_p

Figure 18. Reverse recovery charge Qrr vs. junction temperature

Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 800V and T_J = 25°C

Figure 20. Clamped inductive switching energy vs. junction temperature at V_{DS} = 800V and I_D = 5A

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_g), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the hig

Important notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IM BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.

PART MARKING