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DATASHEET

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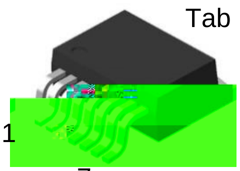
ˆ•‡‡ T ‹ˆ‡ 13,1

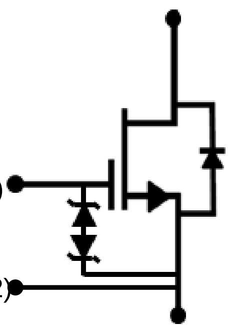
Rev. , !2<!2@Œ 2022

UF3C170400B7S

Description

7KLV 6L&)(7 GHYLFH LV EDVHG RQ D XQLTXH FDVFRGH configuration, FLUFX in which a normally-on SiC JFET is co-packaged with a Si 026)(7 WR SURGXFH D QRUPDOO\ RII 6L&)(7 GHYLFH 7KH GHY GULYH FKDUDFWHULVWLFV DOORZ WKH XVH RI VWDQGDUG JDWH GULYH ,*%7V 6L)(7V 6L& 026)(7V RU 6L VXSHU MXQ Devices. Available in the D^{2}PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive.





Part Number	Package	Marking
UF3C170400B7S	D^{2}PAK-7L	UF3C170400B7S

Features

- On-resistance $R_{DS(on)}$: 410mW (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 70nC
- Low body diode V_{FSD}: 1.5V
- Low gate charge: Q_G = 23.1nC
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3
- AECQ Qualified

Typical applications

- Switching power supplies
- Auxiliary power supplies
- Load switches

Maximum Ratings

Symbol	Value	Units
V_{DS}	1700	V
V_{GS}	-25 to +25	V
	7.6	A
	5.9	A
I_{DM}	14	A
E_{AS}	11.7	mJ
P_{tot}	100	W Td (1

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

		Min	Typ	Max	
BV_{DS}		1700			V
			1.5	60	
			5.5		
I_{GSS}			6	20	mA
			410	515	
			780		
			1070		
$V_{G(th)}$		3	4.7	6	V
R_G			4.1		W

Typical Performance - Dynamic

			Value		Units
			Min	Typ	Max	
Revtsue	C_{iss}			734		
	C_{oss}			13.6		
	C_{rss}			2		
	$C_{oss(er)}$			15.5		pF
	$C_{oss(tr)}$			28		pF
	E_{oss}			11.2		mJ
Total gate charge	Q_G	V_{DS}=1200V, I_D=5A, V_{GS} = 0V to 15V		23.1		nC
Gate-drain charge	Q_{GD}			6.5		
Gate-source charge	Q_{GS}			5.6		
	$t_{d(on)}$	V_{DS}=1200V, I_D=5A, Gate Driver =0V to +15V, $R_{G,EXT}$=50W, Inductive Load, FWD: 2x UJ3D1202TS in series, T_j=150°C		43		ns
	t_r			16		
	$t_{d(off)}$			102		
	t_f			27.5		
	E_{ON}			143		mJ
	E_{OFF}			29		
Total switching energy	E_{TOTAL}			172		
Turn-on delay time	$t_{d(on)}$			33		ns
Rise time	t_r			15		
Turn-off delay time	$t_{d(off)}$			99		
Fall time	t_f			35		
Turn-on energy	E_{ON}			127		mJ
	E_{OFF}			27		
	E_{TOTAL}			154		

Typical Performance Diagrams

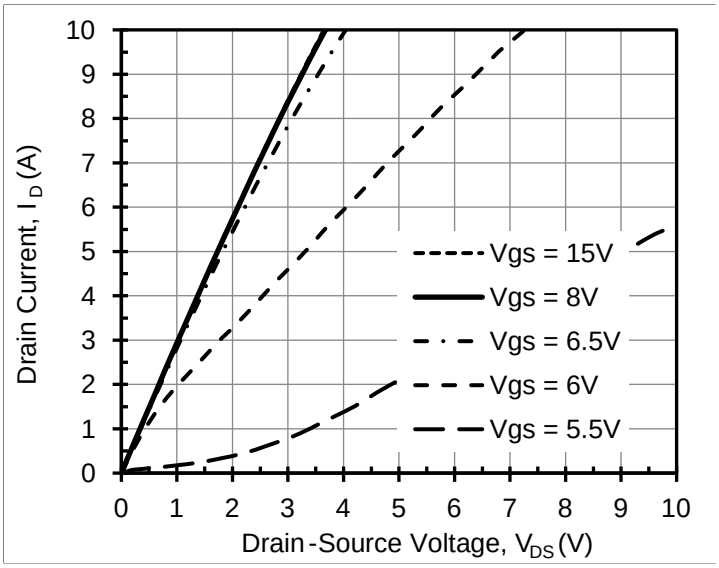


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250ms

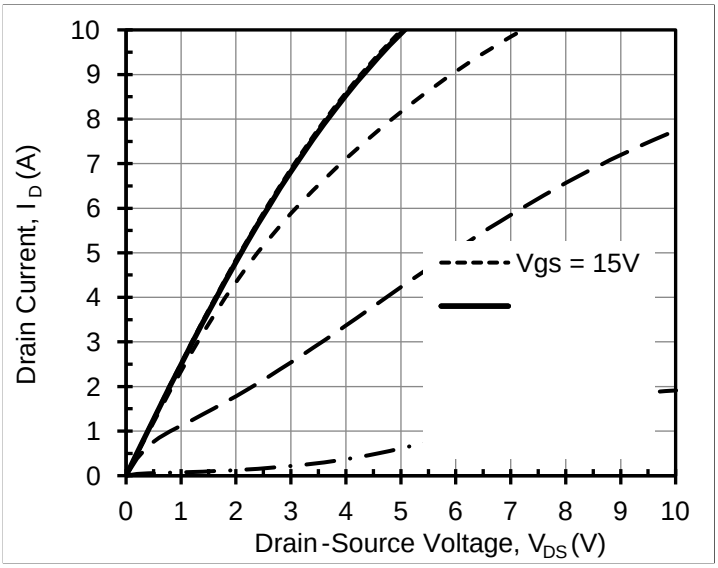


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250ms

Figure 3. Typical output characteristics at T_J = 175°C, tp < 250ms

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 5A

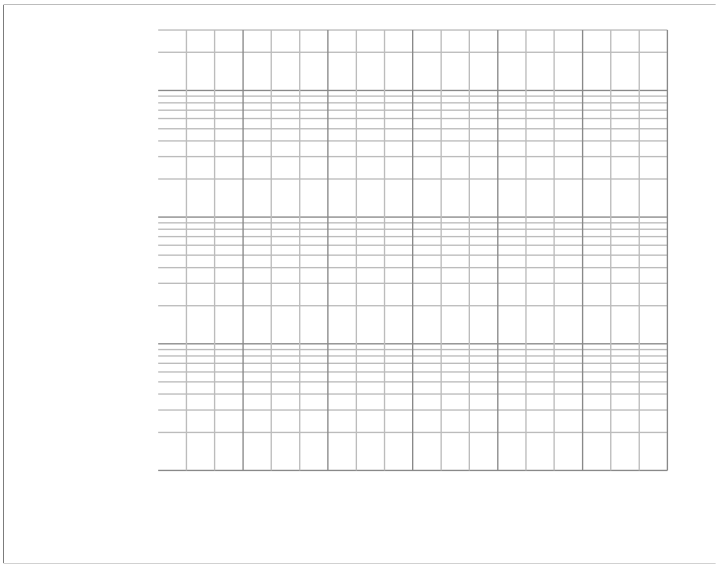


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

Figure 14. DC drain current derating

Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance

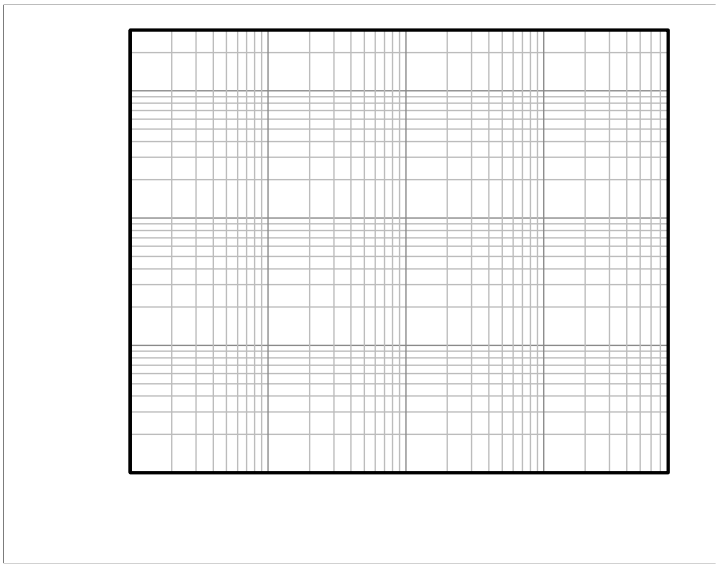


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

Figure 18. Reverse recovery charge Qrr vs. junction temperature

Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 1200V and T_J = 25°C

Figure 20. Clamped inductive switching energy vs. junction temperature at V_{DS} = 1200V and I_D = 5A

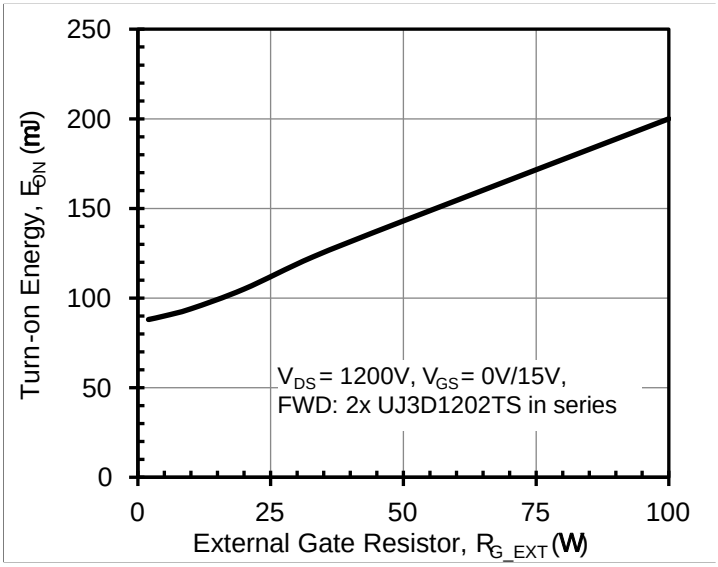


Figure 21. Clamped inductive switching turn-on energy vs. gate resistor R_{G_EXT}

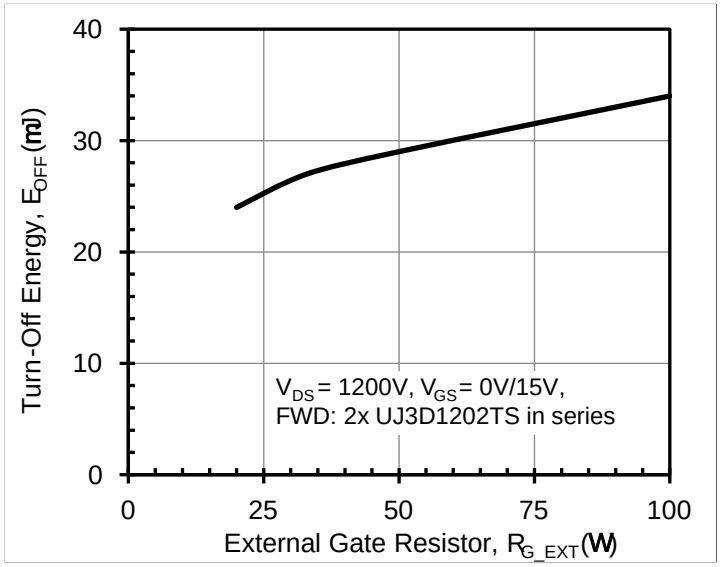


Figure 22. Clamped inductive switching turn-off energy vs. gate resistor R_{G_EXT}

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_g), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the hig dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small R_{G}, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high R_{G} value. There is no extra gate delay time when using the snubber circuitry, and a small R_{G} will better control both the turn-off V_{DS} peak spike and ringing duration, while a high R_{G} will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high R_{G}, while greatly reducing E_{OFF} from mid-to-full load range with only a small increase in E_{ON}. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

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