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DATASHEET

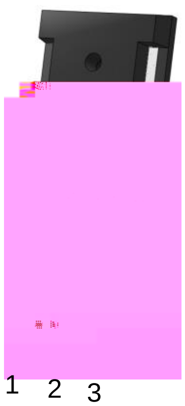
Rev. , January 202 Œ

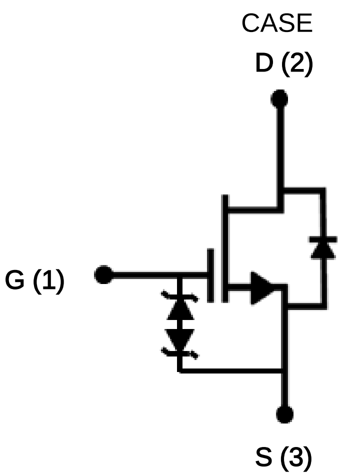
UF3C170400K3S

Description

7KLV 6L&)(7 GHYLFH LV EDVHG RQ D XQLTXH FDVFRGH FLUFXLW configuration , in which a normally-on SiC JFET is co-packaged with a Si 026)(7 WR SURGXFH D QRUPDOO\ RII 6L&)(7 GHYLFH 7KH GHYLFHV VWDQGDUG JDWH GULYH FKDUDFWHULVWLFV DOORZ IRU D WUXH GURS LQ UHSODFHPHQW WR 6L ,*%7V 6L)(7V 6L& 026)(7V RU 6L VXSHUMXQFWLRQ devices. Available in the TO-247-3L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive.

CASE





Features

- Typical on-resistance $R_{DS(on),typ}$ of 410m :
- Maximum operating temperature of 175°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- ESD protected, HBM class 2
- AECQ Qualified

Part Number	Package	Marking
UF3C170400K3S	TO-247-3L	UF3C170400K3S

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1700	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C = 25°C	7.6	A
		T_C = 100°C	5.9	A
Pulsed drain current [2]	I_{DM}	T_C = 25°C	14	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =1.25A	11.7	mJ
Power dissipation	P_{tot}	T_C = 25°C	100	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, ë IURP FDVH IRU VHFRQG\	T_L		250	°C

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	R_{JC}			1.2	1.5	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

		Min	Typ	Max	
BV_{DS}		1700			V
			1.5	60	
			5.5		
I_{GSS}			6	20	A
			410	515	
			1070		
$V_{G(th)}$		3	4.7	6	V
R_G			4.1		

Typical Performance - Reverse Diode

		Min	Typ	Max	
I_S				7.6	A
$I_{S,pulse}$				14	A
			1.5	1.75	
			2.4		
Q_{rr}			70		nC
t					

Typical Performance - Dynamic

	Min	Typ	Max	
C_{iss}		740		
C_{oss}		27		
C_{rss}		2		
$C_{oss(er)}$		15.5		pF
$C_{oss(tr)}$		28		pF
E_{oss}		11.2		J
Q_G		27.5		
Q_{GD}		6.5		
Q_{GS}		10		
$t_{d(on)}$		17		
t_r		13		
$t_{d(off)}$		34		
t_f		27		
E_{ON}		189		

Typical Performance Diagrams

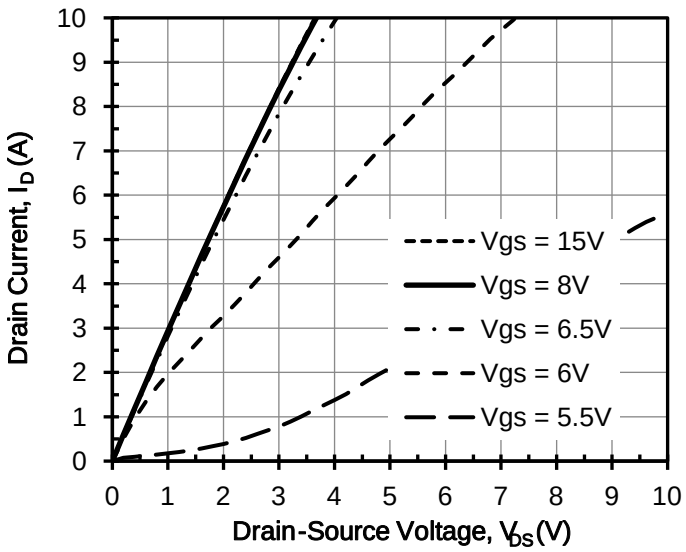


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250 µs

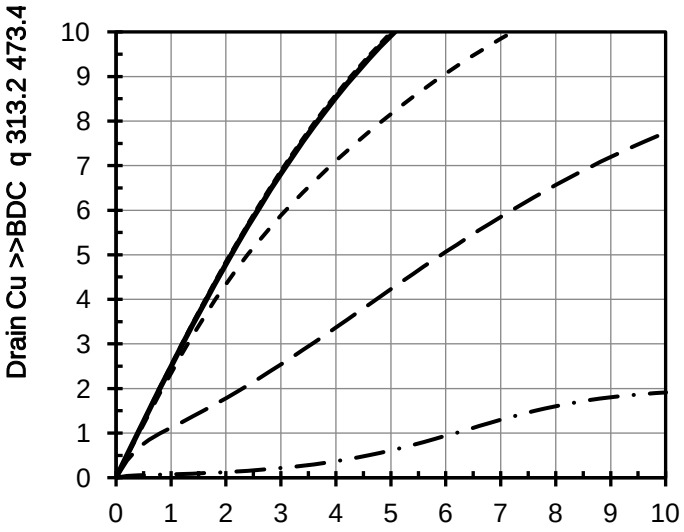


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250 µs

Figure 3. Typical output characteristics at T_J = 175°C, tp < 250 µs

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 5A

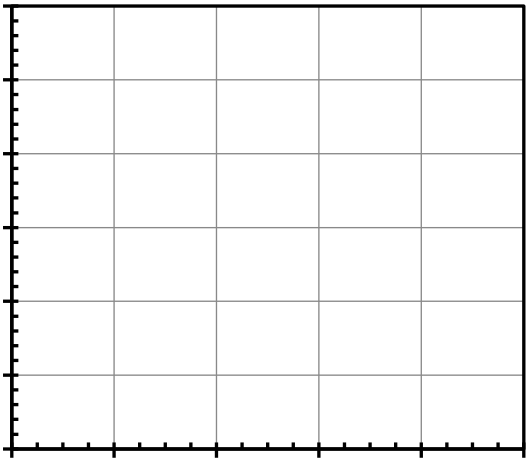


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V

Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

Figure 8. Typical gate charge at V_{DS} = 1200V and I_D = 5A

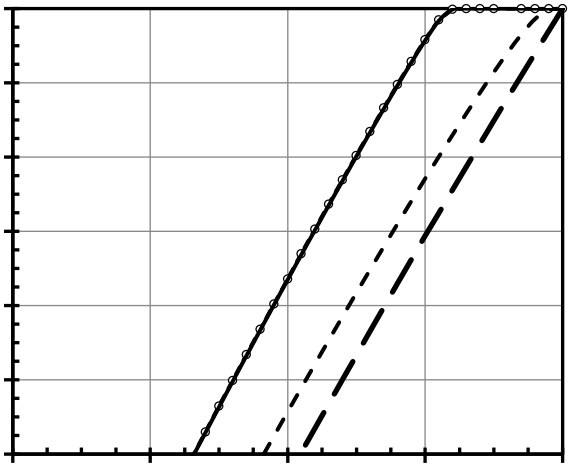


Figure 9. 3rd quadrant characteristics at T_j = -55°C

Figure 10. 3rd quadrant characteristics at T_j = 25°C

Figure 11. 3rd quadrant characteristics at T_j = 175°C

Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

Figure 14. DC drain current derating

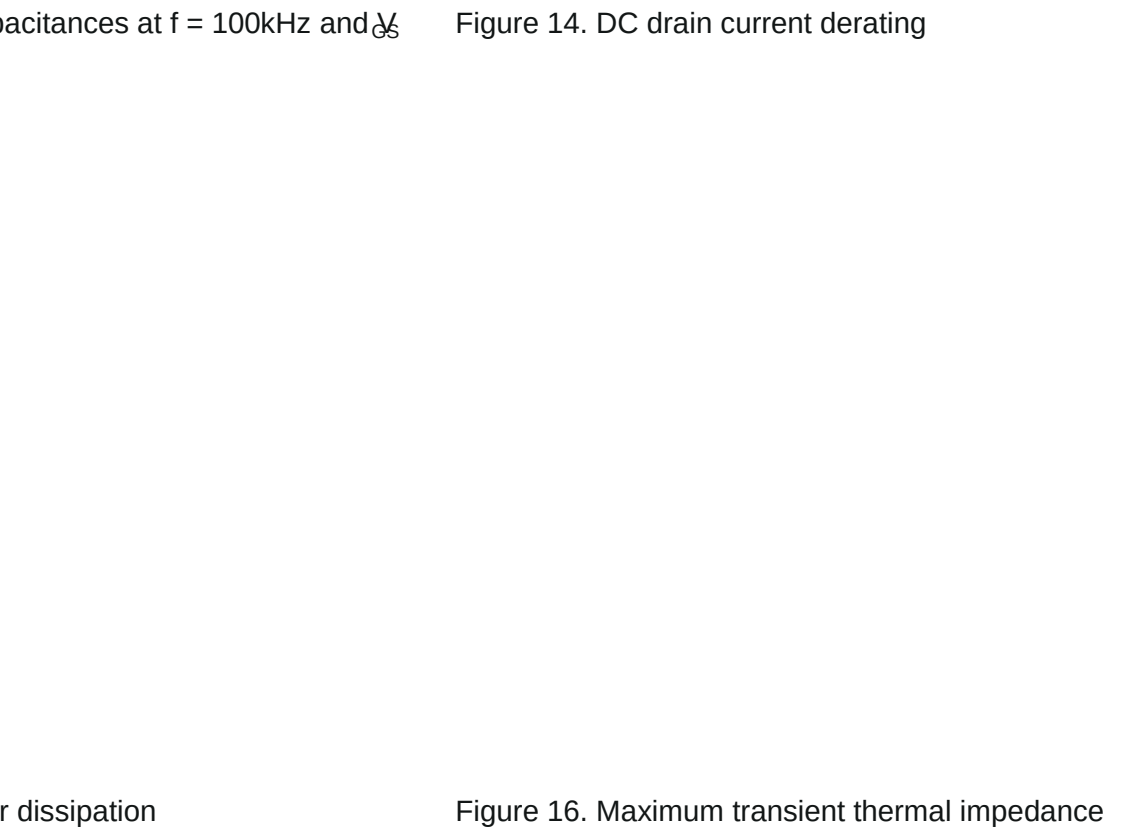


Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance

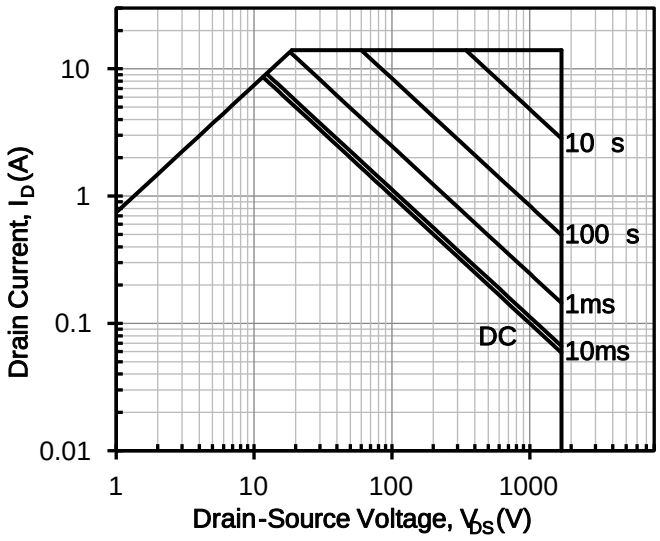


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

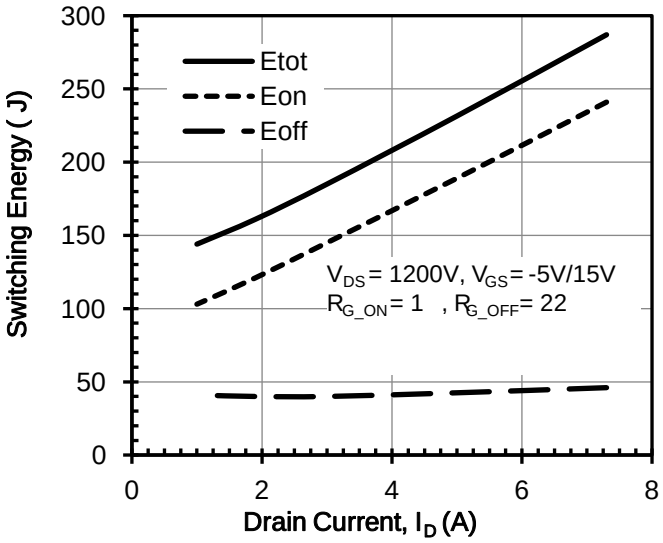


Figure 18. Clamped inductive switching energy vs. drain current at T_J = 25°C

Figure 19. Clamped inductive switching turn-on energy vs. R_{G,EXT_ON}

Figure 20. Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET

Disclaimer

UnitedSiC reserves the right to change or modify any of the products and their inherent physical and technical specifications without prior notice. UnitedSiC assumes no responsibility or liability for any errors or inaccuracies within.

TO-247-3L PACKA OUTLINE, PART MARK AND TUBE SPECIFICAT

PACKAGE OUTLINE

SYM				
	MIN	MAX	MIN	MAX
A	0.185	0.209	4.699	5.309
A1	0.087	0.102	2.21	2.61
A2	0.059	0.098	1.499	