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¤Œ‡ T ‹‰ 13,1

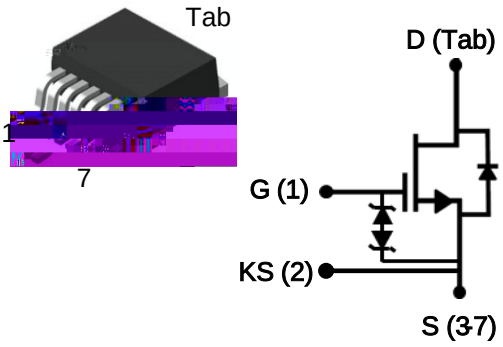
DATASHEET

UF3SC065040B7S

Rev. , ! 2 < !2 8 2 Œ

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D^2PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive.



Part Number	Package	Marking
UF3SC065040B7S	D^2PAK-7L	UF3SC065040B7S

Features

- On-resistance $R_{DS(on)}$: 42m : (typ)
- Operating temperature: 175°C (max)
- ?$'£'2; 8'='89' 8'$3='8@V 88 ' ˆ¥Œ2
- Low body diode V_{FSD}: 1.5V
- Low gate charge: Q_G = 43nC
- Threshold voltage $V_{G(th)}$: 5V (typ) allowing 0 to 15V drive
- Package creepage and clearance distance > 6.1mm
- Kelvin source pin for optimized switching performance
- ESD protected, HBM class 2

Typical applications

Any controlled environment such as

- Telecom and Server Power
- Industrial power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C = 25°C	43	A
		T_C = 100°C	31.5	A
Pulsed drain current [2]	I_{DM}	T_C = 25°C	125	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =3.19A	76	mJ
Power dissipation	P_{tot}	T_C = 25°C	195	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Reflow soldering temperature	T_{solder}	reflow MSL 3	245	°C

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.59	0.77	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	650			V
Total drain leakage current	I_{DSS}	V_{DS}=650V, V_{GS}=0V, T_J=25°C		0.7	150	μA
		V_{DS}=650V, V_{GS}=0V, T_J=175°C		10		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_J=25°C, V_{GS}=-20V / +20V		6	20	μA
Drain-source on-resistanc.[(=2)3.002		V_{GS}=12V, I_D=30A, T_J=25°C		42	52	
				59		
		V_{GS}=12V, I_D=30A, T_J=175°C		78		
	$V_{G(th)}$		4	5	6	V
	R_G			4.5		Ω

Typical Performance - Reverse Diode

			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C=25°C			43	A
Diode pulse current [2]	$I_{S,pulse}$	T_C=25°C			125	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_S=20A, T_J=25°C		1.5	1.75	V
		V_{GS}=0V, I_S=20A, T_J=175°C		1.8		
	Q_{rr}			185		nC
	t_{rr}			31		ns
	Q_{rr}			155		nC
	t_{rr}			30		ns

Typical Performance Diagrams

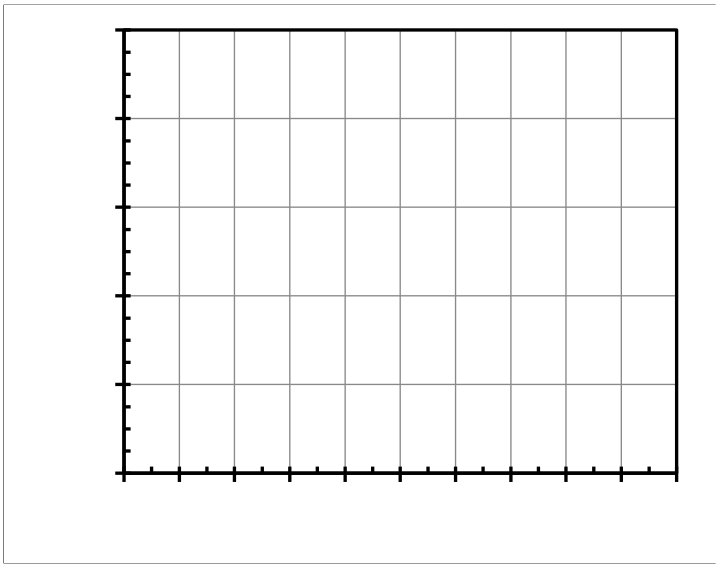


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250 µs

Figure 2. Typical output characteristics at T_J = 25°C, tp < 250 µs

Figure 3. Typical output characteristics at T_J = 175°C, tp < 250 µs

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 30A

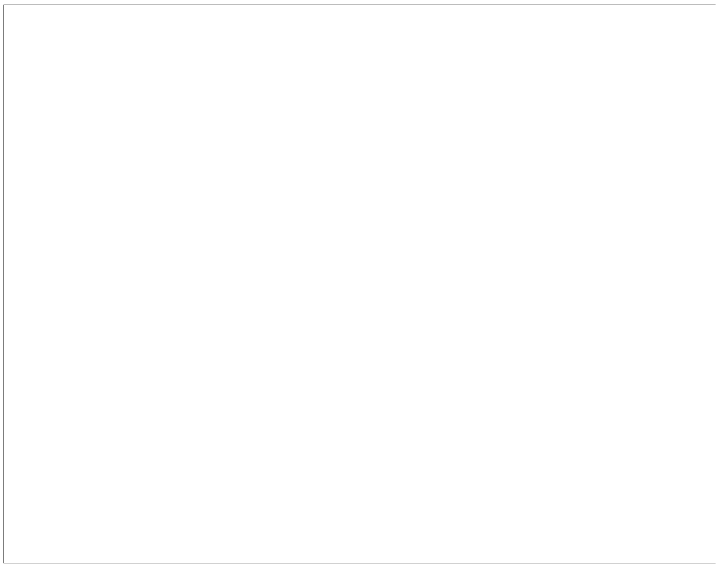


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V

Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

Figure 8. Typical gate charge at V_{DS} = 400V and I_D = 30A

Figure 22: Reverse Recovery Charge Curves

Applications Information

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the hig dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small R_{G}, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high R_{G} value. There is no extra gate delay time when using the snubber circuitry, and a small R_{G} will better control both the turn-off V_{DS} peak spike and ringing duration, while a high R_{G} will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high R_{G}, while greatly reducing E_{OFF} from mid-to-full load range with only a small increase in E_{ON}. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

PART MARKING