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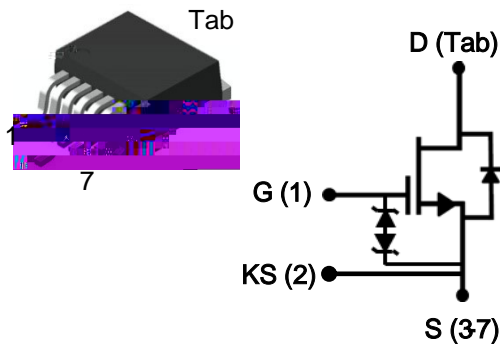
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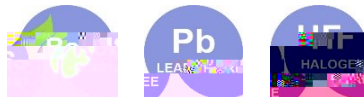


DATASHEET

# UF3SC065040B7S



Part Number	Package	Marking
UF3SC065040B7S	D <sup>2</sup> PAK-7L	UF3SC065040B7S



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## Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D<sup>2</sup>PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive.

## Features

- On-resistance  $R_{DS(on)}$ : 42mΩ (typ)
- Operating temperature: 175°C (max)
- Low body diode  $V_{SD}$ : 1.5V
- Low gate charge:  $Q_g = 43nC$
- Threshold voltage  $V_{G(th)}$ : 5V (typ) allowing 0 to 15V drive
- Package creepage and clearance distance > 6.1mm
- Kelvin source pin for optimized switching performance
- ESD protected, HBM class 2

## Typical applications

- Any controlled environment such as
  - Telecom and Server Power
  - Industrial power supplies
  - Power factor correction modules
  - Motor drives
  - Induction heating



## Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	$V_{DS}$		650	V
Gate-source voltage	$V_{GS}$	DC	-25 to +25	V
Continuous drain current <sup>1</sup>	$I_D$	$T_C = 25^\circ\text{C}$	43	A
		$T_C = 100^\circ\text{C}$	31.5	A
Pulsed drain current <sup>2</sup>	$I_{DM}$	$T_C = 25^\circ\text{C}$	125	A
Single pulsed avalanche energy <sup>3</sup>	$E_{AS}$	$L=15\text{mH}, I_{AS}=3.19\text{A}$	76	mJ
Power dissipation	$P_{tot}$	$T_C = 25^\circ\text{C}$	195	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	$T_J, T_{STG}$		-55 to 175	$^\circ\text{C}$
Reflow soldering temperature	$T_{solder}$	reflow MSL 3	245	$^\circ\text{C}$

1. Limited by  $T_{J,max}$

2. Pulse width  $t_p$  limited by  $T_{J,max}$

3. Starting  $T_J = 25^\circ\text{C}$

## Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{JC}$			0.59	0.77	$^\circ\text{C}/\text{W}$


 Electrical Characteristics ( $T_J = +25^\circ\text{C}$  unless otherwise specified)

## Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	$BV_{DS}$	$V_{GS}=0V, I_D=1mA$ $V_{DS}=650V,$	650	0.7	150	V
Total drain leakage current	$I_{DSS}$	$V_{GS}=0V, T_J=25^\circ\text{C}$ $V_{DS}=650V,$		10		$\mu\text{A}$
Total gate leakage current	$I_{GSS}$	$V_{DS}=0V, T_J=25^\circ\text{C},$ $V_{GS}=-20V / +20V$		6	20	$\mu\text{A}$
		$V_{GS}=12V, I_b=30A,$ $T_J=25^\circ\text{C}$		42	52	
Drain-source on-resistance (= $\approx$ )3.002		$V_{GS}=12V, I_b=30A,$ $T_J=175^\circ\text{C}$		59		
				78		
	$V_{G(th)}$		4	5	6	V
	$R_G$			4.5		$\Omega$

## Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Diode continuous forward current <sup>1</sup>	$I_S$	$T_C=25^\circ\text{C}$			43	A
Diode pulse current <sup>2</sup>	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			125	A
Forward voltage	$V_{FSD}$	$V_{GS}=0V, I_b=20A,$ $T_J=25^\circ\text{C}$		1.5	1.75	V
		$V_{GS}=0V, I_b=20A,$ $T_J=175^\circ\text{C}$		1.8		
	$Q_{rr}$			185		nC
	$t_{rr}$			31		ns
	$Q_{rr}$			155		nC
	$t_{rr}$			30		ns





Typical Performance Diagrams

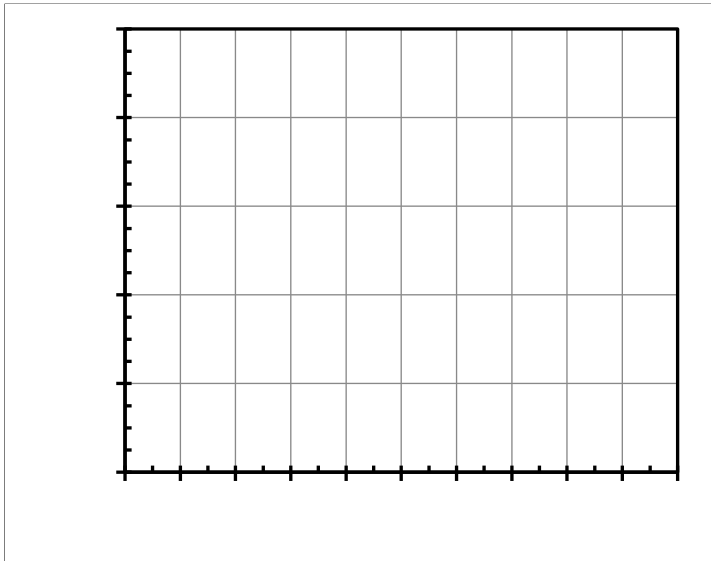


Figure 1. Typical output characteristics at  $T_J = -55^\circ\text{C}$ ,  $t_p < 250 \text{ ns}$

Figure 2. Typical output characteristics at  $T_J = 25^\circ\text{C}$ ,  $t_p < 250 \text{ ns}$

Figure 3. Typical output characteristics at  $T_J = 175^\circ\text{C}$ ,  $t_p < 250 \text{ ns}$

Figure 4. Normalized on-resistance vs. temperature at  $V_{GS} = 12\text{V}$  and  $I_D = 30\text{A}$

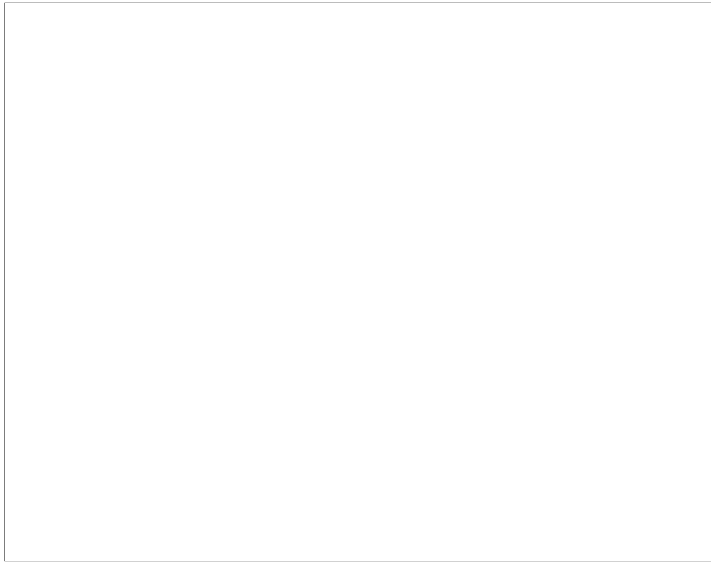


Figure 5. Typical drain-source on-resistances at  $V_{DS} = 12V$

Figure 6. Typical transfer characteristics at  $V_{DS} = 5V$

Figure 7. Threshold voltage vs. junction temperature at  $V_{DS} = 5V$  and  $I_D = 10mA$

Figure 8. Typical gate charge at  $V_{DS} = 400V$  and  $I_D = 30A$



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Figure 22: Reverse (FET) Charge Qrr vs Vds

## Applications Information

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see [www.unitedsic.com](http://www.unitedsic.com).

A snubber circuit with a small  $R_G$ , or gate resistor, provides better EMI suppression with higher efficiency compared to using a high  $R_G$  value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_G$  will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high  $R_G$  will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high  $R_G$ , while greatly reducing  $E_{(OFF)}$  from mid-to-full load range with only a small increase in  $E_{(ON)}$ . Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at [www.unitedsic.com](http://www.unitedsic.com)







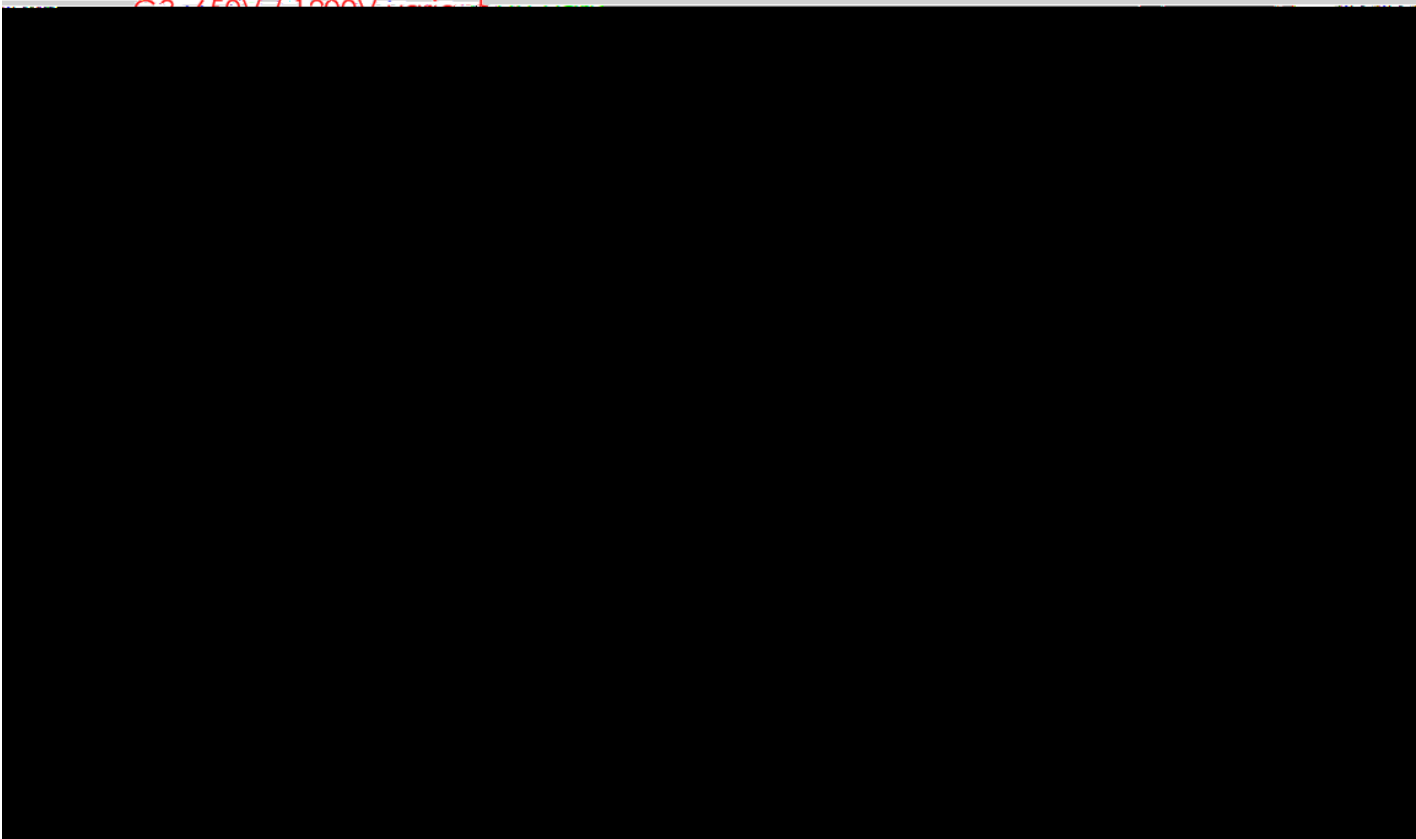
TO263-7L (D2PAK-7L) PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION

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Rev D


PART MARKING



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