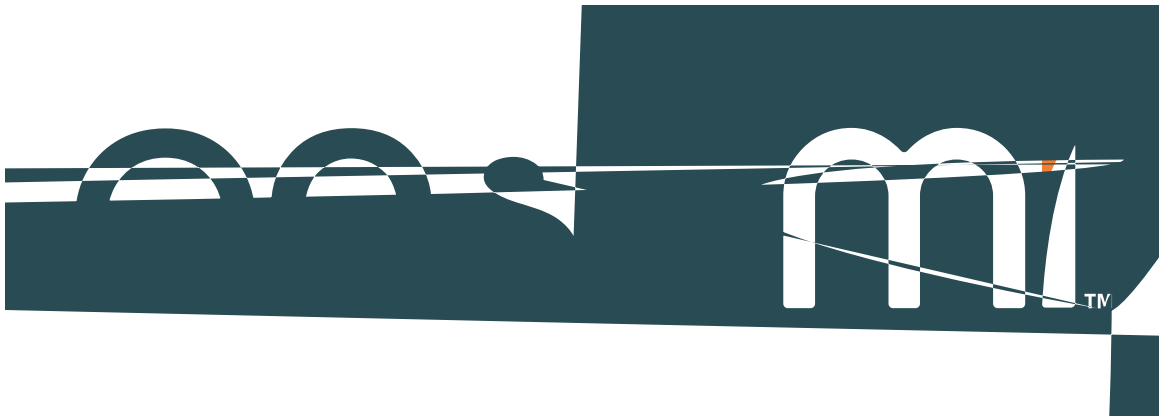


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DATASHEET

UJ3C065030B3

TAB
D (2)

S (3)

| Part Number | Package | Marking |
|--------------|-----------------------|--------------|
| UJ3C065030B3 | D ² PAK-3L | UJ3C065030B3 |

Typical Performance - Dynamic

| | Min | Typ | Max |
|---------------|-----|------|-----|
| C_{iss} | | 1500 | |
| C_{oss} | | 320 | |
| C_{rss} | | 2.3 | |
| $C_{oss(er)}$ | | 230 | pF |
| $C_{oss(tr)}$ | | 520 | pF |
| E_{oss} | | 18.5 | Ⓜ |

Typical Performance Diagrams

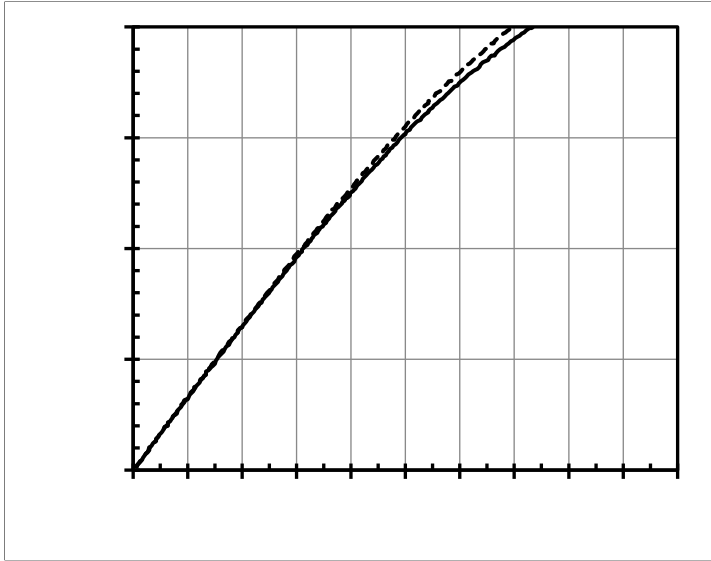


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250 \text{ ns}$

Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250 \text{ ns}$

Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250 \text{ ns}$

Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 50\text{A}$

Figure 10. 3rd quadrant characteristics at $T_J = 25^\circ\text{C}$

Figure 11. 3rd quadrant characteristics at $T_J = 175^\circ\text{C}$

Figure 12. Typical stored energy in C_{SS}

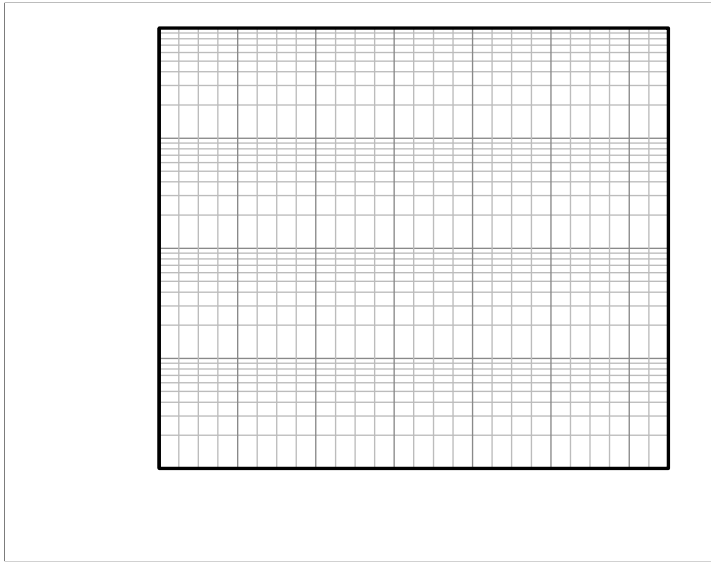


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_G = 0\text{V}$

Figure 14. DC drain current derating

Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance

Figure 17. Safe operation area at $T_J = 25^\circ\text{C}$, $D = 0$,
Parameter t_p

Figure 18. Clamped inductive switching energy vs.
drain current at $T_J = 150^\circ\text{C}$

Figure 19. Clamped inductive switching turn-on
energy vs. R_{θ,EXT_ON}

Figure 20. Clamped inductive switching turn-off
energy vs. R_{θ,EXT_OFF}

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_g), and reverse recovery charge (Q_{rr}).



Important notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein





PARTNUMBER





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