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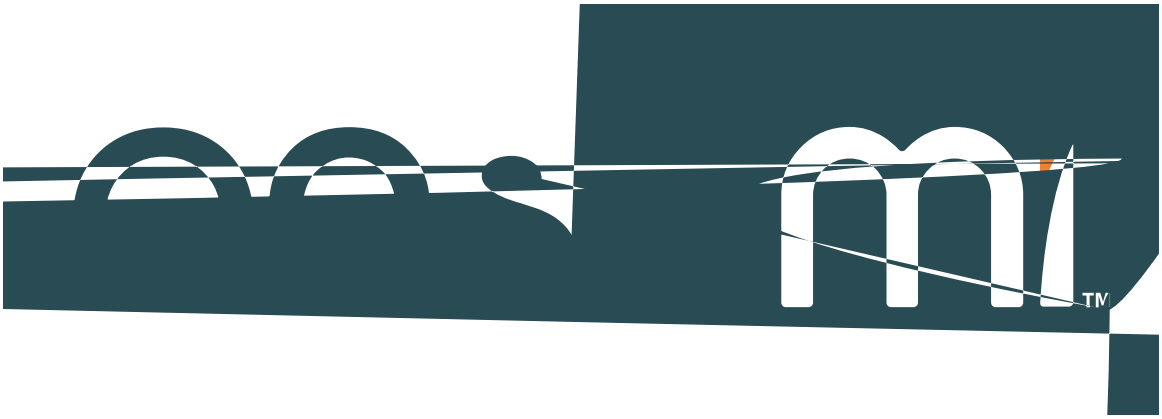

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Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C = 25°C	85	A
		T_C = 100°C	62	A
MEMC ETQq192.31 9.05.17 55.58430.11 648.7 Tc	I_{DM}		230	A
	E_{AS}	L=15mH, I_{AS} =4A	120	mJ
Power dissipation	P_{tot}	T_C = 25°C	441	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8ĩ from case for 5 seconds	T_L		250	°C

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	R_q			0.26	0.34	°C/W

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V f=100kHz		1500		pF
Output capacitance	C_{oss}			320		
Reverse transfer capacitance	C_{rss}			2.3		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=0V		230		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 400V, V_{GS}=0V		520		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=400V, V_{GS}=0V		18.5		mJ
Total gate charge	Q_G	V_{DS}=400V, I_D=50A, V_{GS} = -5V to15V		51		nC
Gate-drain charge	Q_{GD}			11		
Gate-source charge	Q_{GS}			19		
Turn-on delay time	$t_{d(on)}$	V_{DS}=400V, I_D=50A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1W, Turn-off $R_{G,EXT}$=20W Inductive Load, FWD: UJ3D065030TS, T_J=150°C		36		ns
Rise time	t_r			22		
Turn-off delay time	$t_{d(off)}$			56		
Fall time	t_f			15		
Turn-on energy	E_{ON}			472		mJ
Turn-off energy	E_{OFF}			257		
Total switching energy	E_{TOTAL}			729		

Typical Performance Diagrams

Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250ms

Figure 2. Typical output characteristics at T_J = 25°C, tp < 250ms

Figure 3. Typical output characteristics at T_J = 175°C, tp < 250ms

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 50A

Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V

tics at T_J =


Related
Devices


Spice
Models

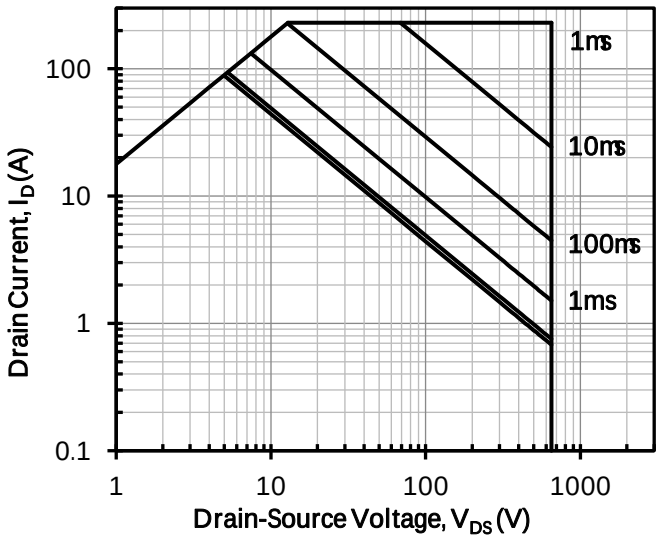

Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

Figure 18. Clamped inductive switching energy vs. drain current at T_J = 150°C

Figure 19. Clamped inductive switching turn-on energy vs. R_{G,EXT_ON}

Figure 20. Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

Figure 21. Clamped inductive switching energy vs. junction temperature at V_{DS} =400V and I_D = 50A

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Disclaimer

TO-220-3L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PART MARKING

PACKING TYPE

ANTI-STATIC TUBE

QUANTITY /TUBE : 50 UNITS

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