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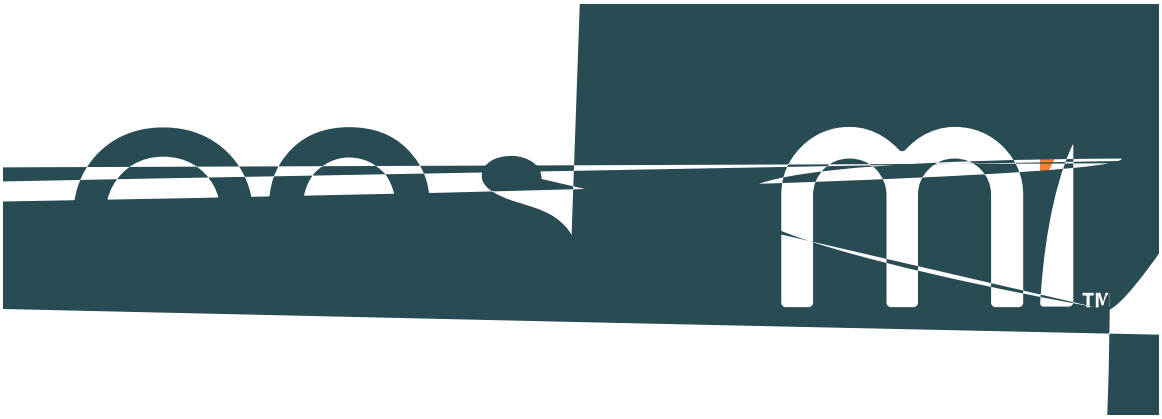

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Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TO-247-3L, 1200 V, 35 mohm

Part Number	Package	Marking
UJ3C120040K3S	TO-247-3L	UJ3C120040K3S

Electrical Characteristics

Typical Performance - Static

Min(T

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V f=100kHz		1500		pF
Output capacitance	C_{oss}			210		
Reverse transfer capacitance	C_{rss}			1.7		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 800V, V_{GS}=0V		112		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 800V, V_{GS}=0V		280		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=800V, V_{GS}=0V		35.6		mJ
Total gate charge	Q_G	V_{DS}=800V, I_D=40A, V_{GS} = -5V to15V		51		nC
Gate-drain charge	Q_{GD}			11		
Gate-source charge	Q_{GS}			19		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=40A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1W, Turn-off $R_{G,EXT}$=20W Inductive Load, FWD: UJ3D1250K T_J=150°C		33		ns
Rise time	t_r			20		
Turn-off delay time	$t_{d(off)}$			63		
Fall time	t_f			20		
Turn-on energy	E_{ON}			930		mJ
Turn-off energy	E_{OFF}			299		
Total switching energy	E_{TOTAL}			1229		

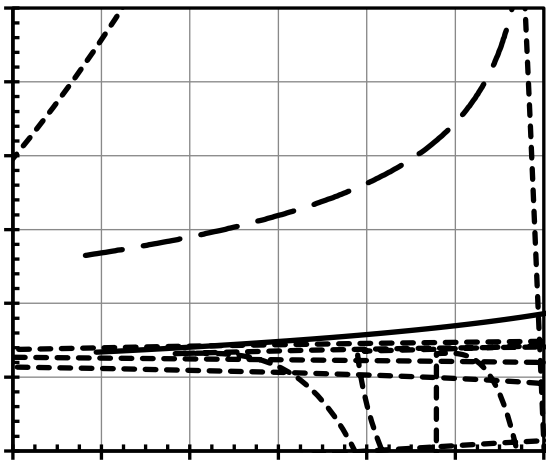

Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

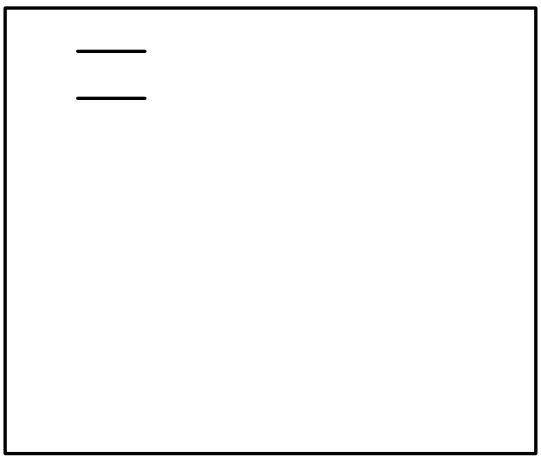

Figure 6. Typical transfer characteristics at V_{DS} = 5V

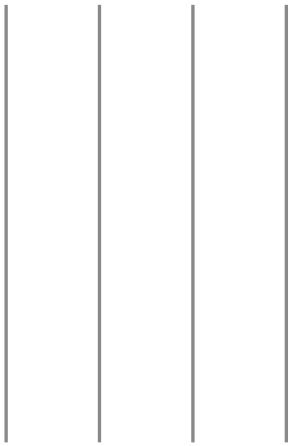

Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

Figure 8. Typical gate charge at V_{DS} = 800V and I_D = 40A

Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

Figure 18. Clamped inductive switching energy vs. drain current at T_J = 150°C

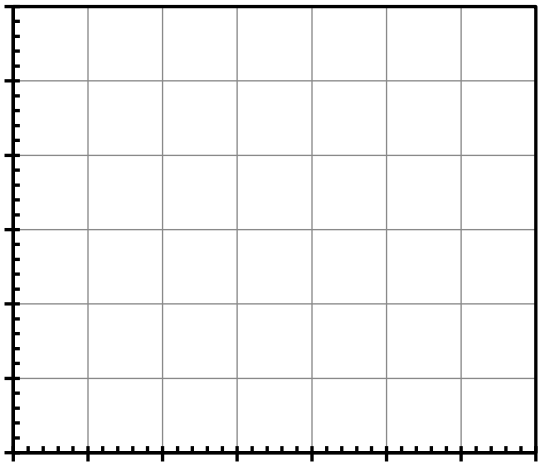

Figure 21. Clamped inductive switching energy vs. junction temperature at V_{DS} = 800V and I_D = 40A

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

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A	0.185	0.209	4.699	5.309
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