NCP1090GEVB, NCP1094GEVB

INPUT SECTION

Ethernet Connectors, Magnetics and Termination



Output Connector

Figure 3. Connection Diagram

The NCP109x evaluation boards have 2 RJ45 connectors. One connector is used as the input connector and supports Power-over-Ethernet. The power from this connector is split off to the NCP109x while the Ethernet data is passed through to the other RJ45 connector. Please note that this second connector will not support Power-over-Ethernet. When the output connector is connected to a proper Power-over-Ethernet PSE, the PD detection will fail without damaging the board, and no power will be applied. When power is applied across the pairs of this second connector without negotiation, the board will burn out the termination resistors.



Figure 4. Ethernet Connection with Power-over-Ethernet

Ethernet connections are double isolated, which means the data passes through a signal transformer on both on the Power Supply Equipment (PSE) side as well as on the Powered Device (PD) side. In the case that the port must support Power-over-Ethernet, specific signal transformers must be selected. First, the signal transformers must have a central tap to access the common mode voltage of each pair, as these are the carriers for the PoE power. Second, care must be taken to select transformers that can support the dc common mode current required (up to 350 mA for the IEEE802.3-af standard and 600 mA for the IEEE802.3-at standard) without high losses. It is recommended to choose magnetics that include common- mode chokes to reduce electromagnetic emissions. When board space is critical, it can be interesting to choose connectors with build-in magnetics ('MagJack'). These connectors also integrate the termination of the Ethernet line. Contact your magnetics manufacturer for more information on magnetics suitable for PoE.

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NCP109x OPERATION

Power-over-Ethernet Detection and Classification

To distinguish power-over-ethernet enabled ports from regular Ethernet ports, the Power Supply Equipment (PSE) will first check the detection signature of the Powered Device (PD), before negotiating and applying power. The detection signature is defined as the resistance between VPORTP and VPORTN, and should be larger than 19 k Ω and smaller than 26.5 k Ω . Typically, a value of 24.9 k Ω is used.

The PSE will measure this resistance by making at least two measurements of the current drawn by the PD while applying voltages between 2.8 and 10 V. From these measurements, the PSE will make a linear approximation from which it will extract the detection resistance.

This means that the total resistance seen at the input of the PD should be equal to 24.9 k Ω . During detection, the DET pin is connected to ground, so for the schematic of the evaluation board, this means that:

$$(R_{UVLO1} + R_{UVLO2}) / / R_{det1} = 24.9 \ k\Omega$$

For the detection and classification to succeed, the total input capacitance of the PD should be limited to less than 150 nF. When the input capacitance is higher, the capacitor charge current will influence the detection resistance measurements, and the detection signature will be invalid. Under no circumstance is it allowed to connect the bulk input capacitor (generally in the order of magnitude of 1-10 μ F) of the DC/DC convertor to VPORTN. The bulk input capacitor should always be located on the other side of the pass switch, and the negative lead should be connected to RTN. As such, the bulk input capacitor will remain disconnected during detection, and will not influence the detection signature.

Once the detection phase is passed, the NCP109x will disconnect the DET pin to save power that would otherwise be dissipated in the detection resistor.

When the PSE has detected a valid PD signature, the PSE will start the classification phase. During the classification phase, the PSE will determine the power class of the PD. This is determined by measuring the current drawn when a voltage pulse of typically 17.5 V is applied. Class 4 is only valid in 802.3at. In 802.3af, class 4 is defined as reserved and treated as class 0. So to make sure that the PD can distinguish between at-type PSEs (applying 25.5 W for class 4) and af-type PSEs (applying 13 W for class 4), the classification pulse is repeated by the at-type PSE when the PD is programmed for class 4. This difference is made visible to external components through the nClassAT pin.

The power class can be programmed by setting the classification resistor to the correct value. Programming resistors should be placed as close to the IC as possible to minimize noise. The different power classes and their corresponding classification resistors are listed in Table 2.

Power Class	Average Input Pow- er of the PD	Classification Resistor		
0	13 W	4.42 kΩ		
1	3.84 W	953 Ω		
2	6.49 W	549 Ω		
3	13 W	357 Ω		
4*	25.5 W	255 Ω		

Table 2. PD POWER CLASSIFICATION

*Only for NCP1093, NCP1094

After the PSE has detected a valid power class for the PD, it will apply the full power to the PD.

A typical classification sequence for at7 5esistor.

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Inrush and Operational Current Limitation

When the PSE applies power to the PD after the detection and classification phases, the pass switch will initially limit the current passing through it. In this way large currents caused by the DC/DC convertor input capacitor charging are prevented.

When the voltage over the pass switch drops below the limit value, this indicates that the bulk capacitor is charged.

Table 3. PD INPUT CURRENT LIMITS

The pass switch is then turned completely on, and the IC switches to an operational current limit. Both limits are programmed with the same programming resistor, which is connected to ILIM. Programming resistors should be placed as close to the IC as possible to minimize noise. Typical values for this programming resistor are shown in Table 3.

Average Input Power of the PD	Recommended ILIM Resistor	Inrush Current Limit	Operational Current Limit
13 W	178 kΩ	120 mA	500 mA
25.5 W	169 kΩ	120 mA	680 mA

PGOOD Indication

The NCP109x provide a PGOOD signal to indicate when the power is available for the DC/DC convertor. This is an open-drain output that is active when the input capacitor has not completely charged yet. The PGOOD pin is released (to an external pull-up) when the voltage between RTN and VPORTN drops below 1 V (typ.).

The intended use for this signal is to connect the PGOOD signal to the enable pin of your DC/DC controller, to ensure that the DC/DC controller does not start operation before the input capacitor is fully charged.

On the evaluation board the PGOOD pin is connected to a LED. Under normal operation, this LED should only turn

source was connected first. For example, when the auxiliary is already connected when the Ethernet cable is plugged in, the auxiliary voltage will interfere with the PoE detection, and this will result in a dominant auxiliary supply. However, if the Ethernet cable is connected first, the PoE detection will be successful, and power will be drawn from the PoE interface, even if an auxiliary supply is later connected.

It is often desirable for the device to always use the auxiliary supply, even when PoE is available. In that case, the PoE must be disabled when the auxiliary is active. This

Auxiliary support will disconnect the PoE supply when an

UVLO,off

 $\frac{1}{R_{2vlo}} + R}{R_{2vlo}}$

Take also into account that the UVLO resistors will influence the detection resistance.

undo

An auxiliary supply can easily be implemented with a diode (Daux1). This auxiliary supply is often of a relatively low voltage (e.g. 24 V). However, this implementation can result in variable behavior, depending on which power

to flow through the auxiliary resistor divider, the AUX pin voltage would rise above the threshold, and turn of the PoE, even when no auxiliary supply is available. For this reason,

we put a PNP transistor (Q1) in series, which will disable this current path. The resulting schematic is shown in Figure 9.



Figure 9. Auxiliary Supply Circuit

nClass_AT

The NCP1093 and NCP1094 are capable of classifying as

class 4 as per the 802.3at standard, delivering up .ulfyi 0 PE939 Tc2ys3, CP1/TT4 - 3.071 J62 TD-.003 Tc0 Tw TD-.0er tlf802.3PDhowncor

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