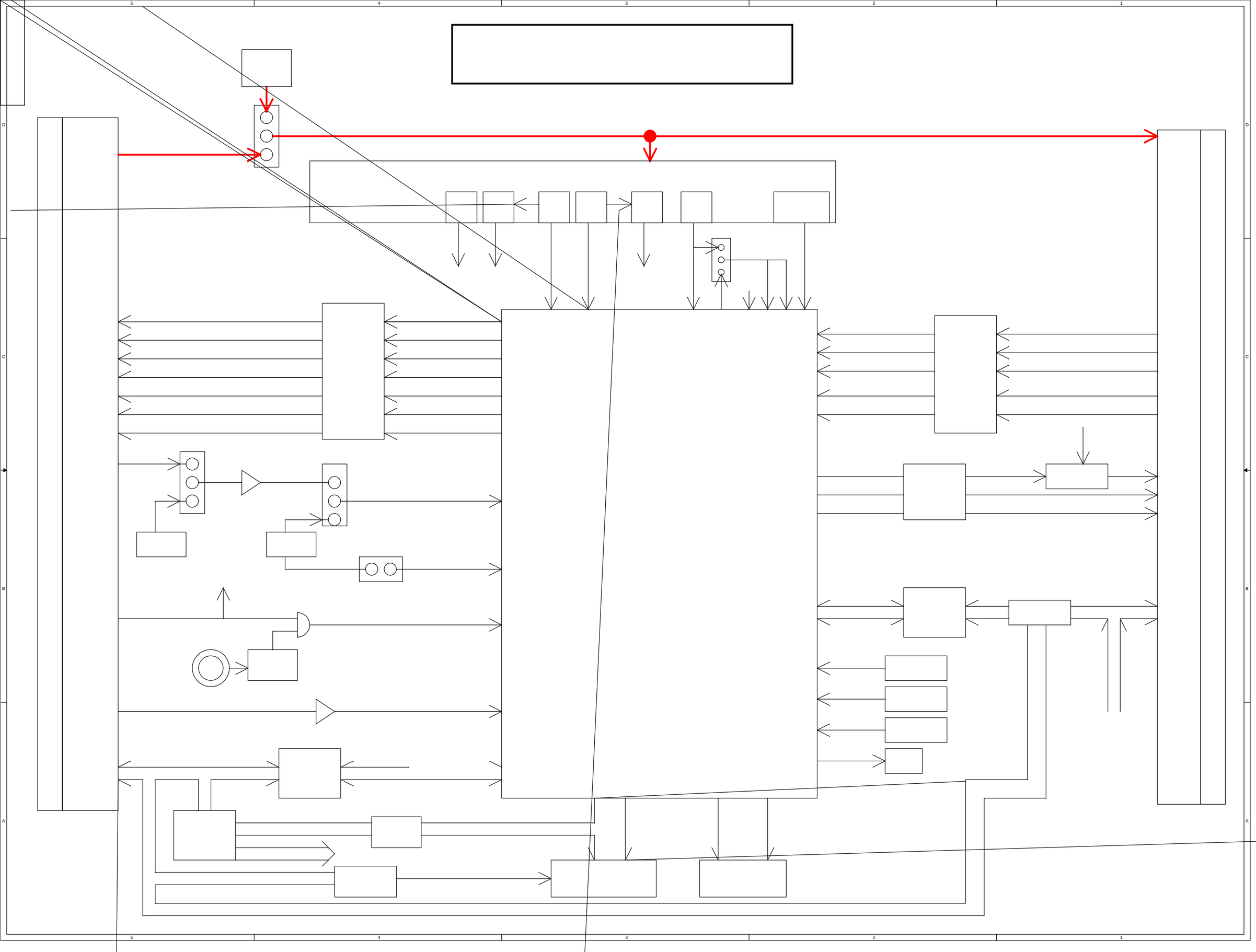
AP0101_81BGA_Adapter_Rev2

5	Clock and Reset
6	External Interfaces

Rev	Who	Date	Description
Rev 0.0	W.B.Foo	06/20/11	Initial.
Rev 0.1	W.B.Foo	08/18/11	Add P5, P51 and P19
Rev 0.2	W.B.Foo	08/19/11	Add U20, R63, Q1 and change P29 to polarized type type connector
Rev 0.3	W.B.Foo	08/23/11	Add P30, P31, P52, P53, R63, Q2, Q3, P8 and R55
Rev 1.0	W.B.Foo	10/10/11	Change Level Translator U11/U12 from PCA9517 to TXB0102 & R24/R25 to 2.2K resistor on Pg 5
Rev 1.1	W.B.Foo	10/28/11	Change test point TP6/TP7/TP8/TP11/TP10 to through hole type
Rev 1.2	W.B.Foo	12/19/11	1) Change U16/U24 to single part of U24(SN74AVCH4T245) combine M_TRIG/MCLK_OUT/RST_N_OUT 2) Add power supply for FPGA +1V2_VCCINT/+2V5_VCCA/+VCCIO/+3V3_HVCCIO 3) Add FPGA U32 & Flash Memory U47



AP0101 IC

P19:
Short 1-2 (Default)

P19:
Close -> Default

P4 (SADDR):
Pins 2-3(GND) I2C Addr --> 0x90 (default)
Pins 1-2(+HVDDIO) I2C Addr --> 0xBA

SADDR

HCLK_IN
H_SCL
H_SDA
H_RST_N
SENIN_D[11:0]
SENIN_D0
SENIN_D1
SENIN_D2
SENIN_D3
SENIN_D4
SENIN_D5
SENIN_D6
SENIN_D7
SENIN_D8
SENIN_D9
SENIN_D10
SENIN_D11

RST_N_OUT
H_DATA[15:0]
H_DATA0
H_DATA1
H_DATA2
H_DATA3
H_DATA4
H_DATA5
H_DATA6
H_DATA7
H_DATA8
H_DATA9
H_DATA10
H_DATA11
H_DATA12
H_DATA13
H_DATA14
H_DATA15

P6 (STANDBY) Tri-stage:
Pins 2-3(GND) --> Standby mode
Pins 1-2(+3V3) --> Active mode (default)
Open -> Auto Control by serial

STANDBY

XTAL2
SENIN_FV
SENIN_LV
SENIN_PIXCLK
H_FV
H_LV
H_PIXCLK
MCLK_OUT
M_TRIG

P3:
Short 2-3 (Default)

HF_SYNC
M_SCL
M_SDA

P8 (GPIO1_LED):
Pins 2-3 --> Set to GPO
Pins 1-2 --> Set to GPI

SPI_SDI
(DNL)
SPI_CS_N
SPI_SCLK
SPI_SDO

(DNL)

SPI PROGRAMMING CONNECTOR

P7 (SPI Memory Selection):
Jumper 2-3 -> FLASH disable
Jumper 1-2 -> EEPROM disable

SPI EEPROM
(1Mbit)

HOST Mode**(Default)**
P5 = Short 1-2/P45 = Open => SPI_SDI = GND

FLASH Mode
P5 = Open/P45 = Open => SPI_SDI = Flash/EEPROM Data

AUTO Config Mode
P5 = Short 1-2/P45 = Short 1-2 => SPI_SDI = High Impedance

Serial Control
P5 = Open/P45 = Open => SPI_SDI = Serial control mode type

Device Address:0x82

SPI FLASH
(512Kbit)

5 4 3 2 1

External Interface

Demo2X I/F

Demo2X I/F

Parallel Data Level Shifter
(HeadBoard -> AP0101 board)

nOE	DIR	Operation
L	L	B --> A
L	H	A --> B
H	X	Isolation

BEAGLE/FPGA EXT I/F

BEAGLE I/F

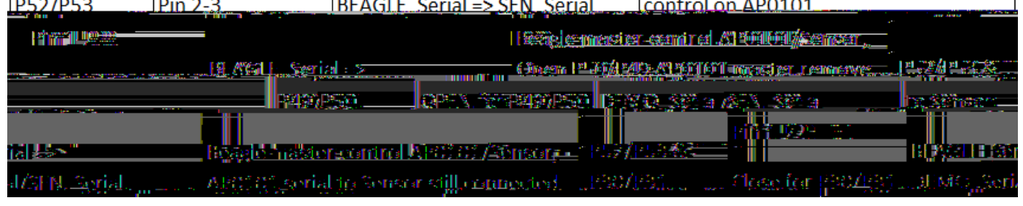
P30
Open --- DEMO2X & Sensor NO accessed (Default)
Closed --- DEMO2X & Sensor accessed

P52
Pins 1 - 2 --- DEMO2X accessed (default)
Pins 2 - 3 --- Sensor accessed Only

P31
Open --- DEMO2X & Sensor NO accessed (Default)
Closed --- DEMO2X & Sensor accessed

P53
Pins 1 - 2 --- DEMO2X accessed (default)
Pins 2 - 3 --- Sensor accessed Only

Beagle Serial configuration			
Header	Pin condition	Signal connection	Remark
P52/P53	Pin 1-2	BEAGLE_Serial => DEMO_Serial	Beagle master control AP0101, Remove R58/R57 DEMO2X master remove
P52/P53	Pin 2-3	BEAGLE_Serial => SEN_Serial	Beagle master control Sensor, no control on AP0101



FPGA Interface

H_DATA9
H_DATA7

H_DATA11

H_DATA10
H_DATA8
H_FV
H_LV

H_DATA12

H_DATA6
H_DATA5
H_DATA4

H_DATA0

GPIO3_D17

GPIO4_D18
H_DATA3
H_DATA1

GPIO5_D19

GPIO2_D16

H_DATA2

H_PIXCLK

H_DATA15
H_DATA14
H_DATA13

DEMO_LV

DEMO_D11
DEMO_D8

DEMO_D15
DEMO_D12
DEMO_FV
DEMO_D1
DEMO_D6
DEMO_D7
DEMO_D2

DEMO_D5
DEMO_D10
DEMO_D4
DEMO_D9

DEMO_D13

(DNL) **(DNL)**

(DNL)

AS Mode	MSEL2	MSEL1	MSEL0	Remark
Standard	0	1	0	Default
Fast	0	0	0	

Beagle Serial configuration			
	Pin 1-2		still connected
	Close for P30/P31		Beagle master control AP0101/Sensor, Open P50/P49 AP0100
P31	OPEN for P49/P50	BEAGLE_Serial => DEMO_Serial/SEN_Serial	master remove to Sensor
to-configuration			
eader	Pin condition	Signal Condition	Remark
3/P44	P44 = Short 1-2/P43 = Short 1-2	Disable U30/U29	Beagle no access to
	P5 = Short 1-2/P45 = Open	Host Mode (SPI_SDI = GND)	SPI_SDI Table:
	P5 = Open/P45 = Open		