



TSOP i6 3.00x1.50x0.90, 0.95P  
CASE 318G  
ISSUE W

DATE 26 FEB 2024

NOTES:

1. DIMENSIONING AND TOLERAN

TSOP i6 3.00x1.50x0.90, 0.95P  
CASE 318G  
ISSUE W

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GENERIC  
MARKING DIAGRAM\*



XXX = Specific Device Code  
A =Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

STYLE 1:

- PIN 1. DRAIN
- 2. DRAIN
- 3. GATE
- 4. SOURCE
- 5. DRAIN
- 6. DRAIN

STYLE 2:

- PIN 1. EMITTER 2
- 2. BASE 1
- 3. COLLECTOR 1
- 4. EMITTER 1
- 5. BASE 2
- 6. COLLECTOR 2

STYLE 3:

- PIN 1. ENABLE
- 2. N/C
- 3. R BOOST
- 4. Vz
- 5. V in
- 6. V out

STYLE 4:

- PIN 1. N/C
- 2. V in
- 3. NOT USED
- 4. GROUND
- 5. ENABLE
- 6. LOAD

STYLE 5:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. COLLECTOR 1
- 4. EMITTER 1
- 5. BASE 1
- 6. COLLECTOR 2

STYLE 6:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. EMITTER
- 5. COLLECTOR
- 6. COLLECTOR

STYLE 7:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. N/C
- 5. COLLECTOR
- 6. EMITTER

STYLE 8:

- PIN 1. Vbus
- 2. D(in)
- 3. D(in)+
- 4. D(out)+
- 5. D(out)
- 6. GND

STYLE 9:

- PIN 1. LOW VOLTAGE GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN
- 5. DRAIN
- 6. HIGH VOLTAGE GATE

STYLE 10:

- PIN 1. D(OUT)+
- 2. GND
- 3. D(OUT)-
- 4. D(IN)-
- 5. VBUS
- 6. D(IN)+

STYLE 11:

- PIN 1. SOURCE 1
- 2. DRAIN 2
- 3. DRAIN 2
- 4. SOURCE 2
- 5. GATE 1
- 6. DRAIN 1/GATE 2

STYLE 12:

- PIN 1. I/O
- 2. GROUND
- 3. I/O
- 4. I/O
- 5. VCC
- 6. I/O