NIS5135, NIS5132 and NIS5232 Enable/Fault Pin

The enable pin of the NIS5135, NIS5132, and NIS5232 has three different logic levels. T

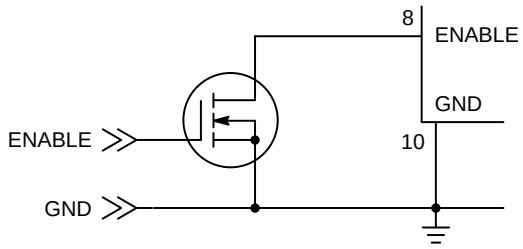
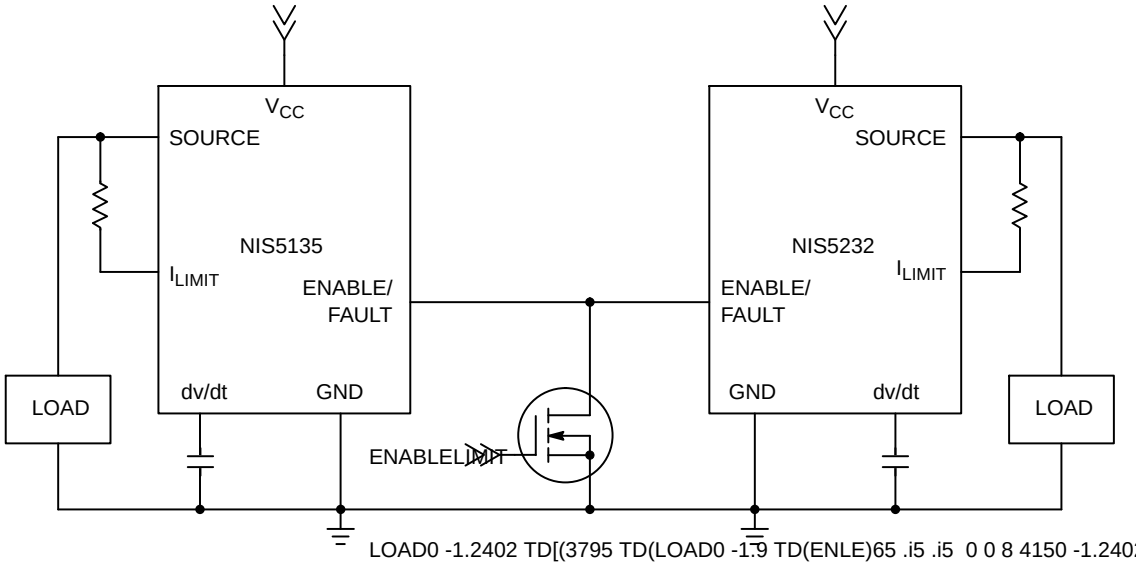


Figure 3. Circuit for Forcing a Low State on the Enable Pin

Activation of the thermal shutdown circuit provides a high signal to the internal thermal shutdown transistor to pull the enable pin out of the high state. A 1.4 V diode drop element in series with the internal thermal shutdown transistor results in the enable pin being pulled to the intermediate or mid state. Since the mid state is below the trip point for the enable SD comparator, a high enable SD is generated and the eFuse output is disabled.

An alternate method of controlling the state of the enable pin is to tie the enable pins of multiple eFuses together. The maximum fanout (the total number of eFuses that can be connected to the pin for simultaneous shutdown) is three. A common application is a system with 5 and 12 V rails using the NIS5135 and the NIS5232 with the enable pins connected to each other as shown in Figure 4. With multiple enable pins tied together a thermal fault on one eFuse forces a mid level on all of the eFuses. This ensures full shutdown of a system under a thermal fault condition on any of the eFuses.



Summary

The enable pin of ON Semiconductor eFuses provides a number of features. With all eFuses, a transistor may be used to force the pin low to disable the output. In addition, it may be left floating if no control of the enable pin is required. With thermal latching eFuses, it may be brought low and then allowed to go high to reset the device. The enable pin of the NIS5135, NIS5132, and NIS5232 has a middle logic state and their enable pins may be connected to allow a common thermal shutdown. A capacitor may be connected on the NIS5112 to serve as a startup timer, while the NIS5135, NIS5132MN1, NIS5132MN2, and NIS5232 have an internal startup blanking circuit and should not have a capacitor connected from the enable pin to ground.