

# POWER WEBINAR

## 2022 Power Webinars Abstracts

**Power Electronics: Silicon Carbide (SiC) Power MOSFETs**

Date: Tuesday, October 18 at 10:00 a.m. CET and PST

Author: Catherine De Keukeleire

[Silicon Carbide \(SiC\)](#) can be considered one of the most promising semiconductor materials for manufacturing high-power electronic devices. Thanks to its excellent physical properties (high saturation electron drift velocity, high thermal conductivity, high breakdown electric field), systems with very low losses and faster switching speed can be designed. Smaller geometries can be designed. This session will introduce the audience to the

**onsemi** Quality and Reliability methodology deployed from first design to mass production. This comprehensive approach is founded on the interaction between different fields, such as a rigorous design methodology, strict production monitoring, manufacturing control, adequate screening, and robust qualification plans. This methodology has shown its efficiency on silicon products applied to the automotive market for many decades and has been tailored to address the specific needs of SiC products. You will be guided through this evolution to SiC and, more specifically, on its successful deployment to address the integrity of the gate oxide of SiC MOSFET transistors.

Finally, the webinar will briefly present recent publications on Cryogenic Bias Temperature Instability, Body Diode degradation, and Dynamic stress requirements.

**Lessons Learned from 25 kW DC Charging Modules**

Date: Wednesday, October 19 at 10:00 a.m. CET and PST

Authors: Didier Balocco, Daniel Goldmann, Stefan Kosterec, Karol Rendek

[In our eight-part how2power blog series](#), we described the development of a [25 kW DC charging module](#) in detail. In this webinar, we will focus on Tips and Tricks from the HW and FW design perspective and debugging phase to share 25 kW DC charging module development and testing hints. We will explain how to test and fine-tune short circuit desaturation protection and what causes [SiC MOSFET](#) drain voltage ringing. We will show the impact of adding a snubber capacitor and how to test Device Under Test (DUT) with lower power equipment than the power of tested DUT in a loop-back test. Finally, we will touch on Phase Shifted Dual Active Bridge control algorithm design.

**Physical and Scalable SPICE Simulation Models**

Date: Thursday, October 20 at 10:00 a.m. CET and PST

Author: Didier Balocco

In last year's sessions, we explained how **onsemi** [Physical and Scalable SPICE Simulation Models](#) are made and used to obtain data sheet values. In this session, however, we will focus on results that can be obtained only by simulation and how to use them in some high-power conversion topologies.

The session's first part will explain

- How to access internal node voltage or the die voltage
- How to use corner simulation models to study current sharing between MOSFETs in parallel
- How to use the thermal interface with a cauer network
- How package parasitics can influence switching losses
- How a half-bridge structure can also affect losses

The session's second part will focus on topologies simulations including

- Flying Capacitor Boost
- NPC and T-NPC cells
- 6-Pack Boost Active Front End with complete D-Q control and 3rd Harmonic Injection

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